

Model Name :

File Name :

# Compal Confidential

## *ULC UMA M/B LA-A994P Schematics Document*

Intel Bay Trail M VC

Project Code : ZSO50

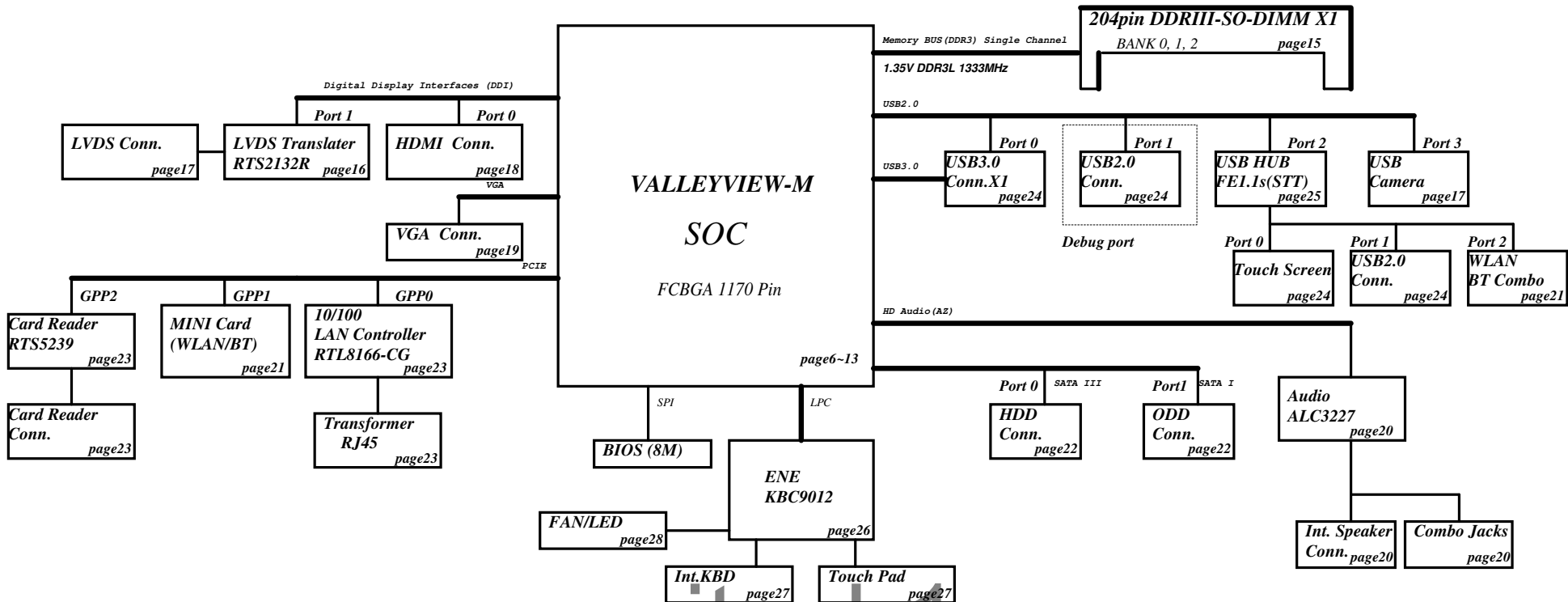
2014/02/05

MV Rev. 1.0

DAX ZSO50 BayTrail-M

Part Number	Description
DAZ14Z00200	PCB 14Z LA-A994P REV0 M/B 4

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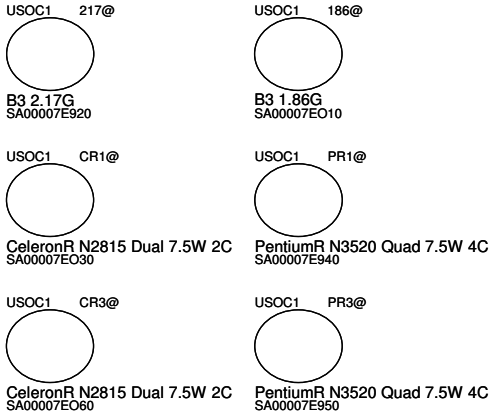
Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.2VALW	+1.2v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

BOARD ID Table

Board ID	PCB Revision
DB	0.1
SI	0.2
PV	0.3
MV	1.0

BOM Option Table	
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMI requirement	EMI@
EMI requirement unpop	@EMI@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
8161 LAN controller	8161@
8166 LAN controller	8166@
LVDS	LVDS@
LVDS LDO mode	LVDSLDO@
LVDS SWR mode	LVDSWR@
Translator RTS2132S	2132S@
Translator RTS2132R	2132R@
Short Pad	RS@
Clean CMOS	CMOS@
Jump	JP@



EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

SOC SM Bus address

Device	Address
ChannelA DIMM0 A0	1010 000X JDIMM1(SPD)

43 level BOM table

43 Level	Description	BOM Structure
4319P6BOL01	SMT MB AA231 V1UE3 HDMI	

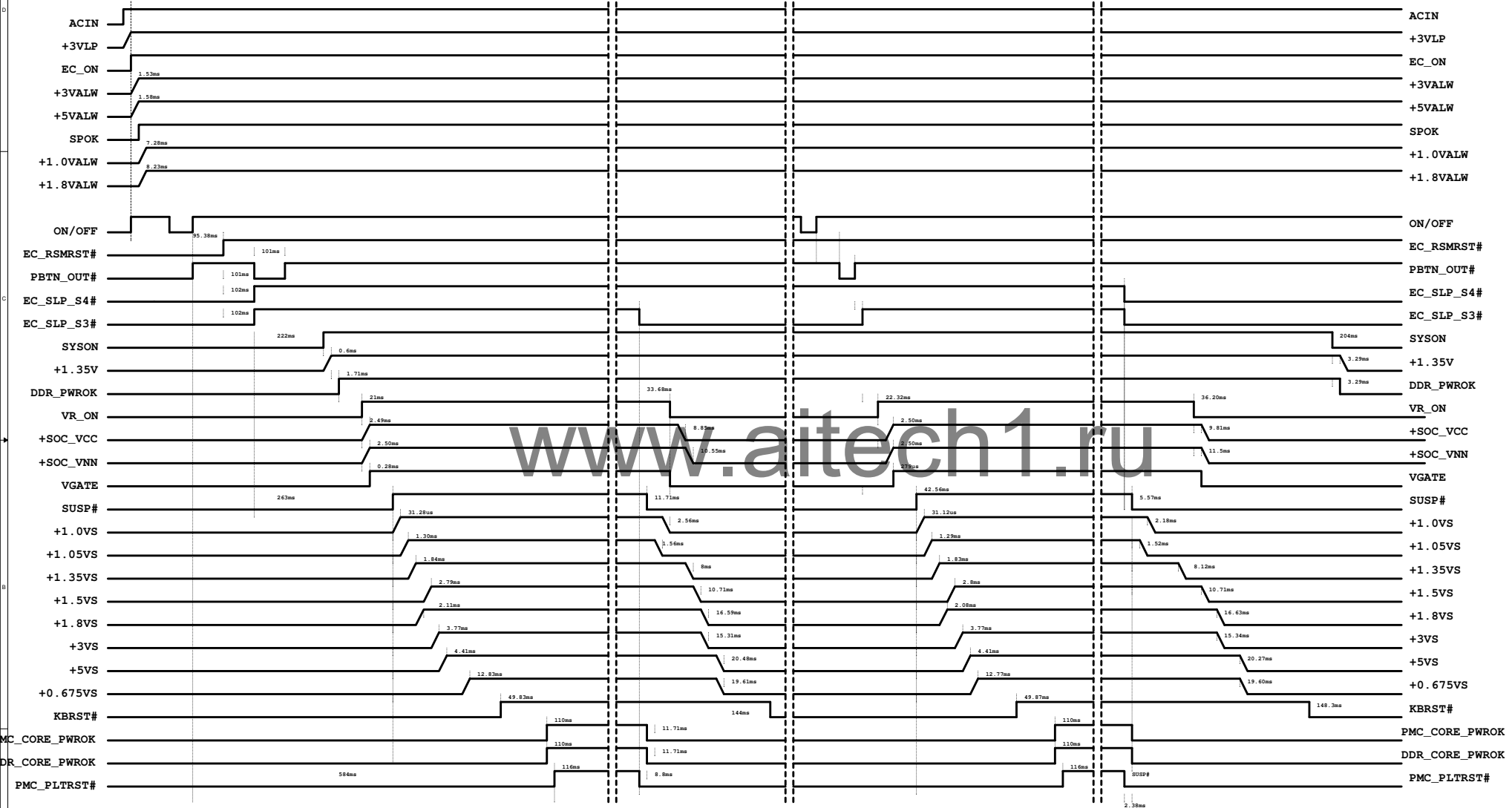
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G3-&gt;S0

S0-&gt;S3

S3-&gt;S0

S0-&gt;S5

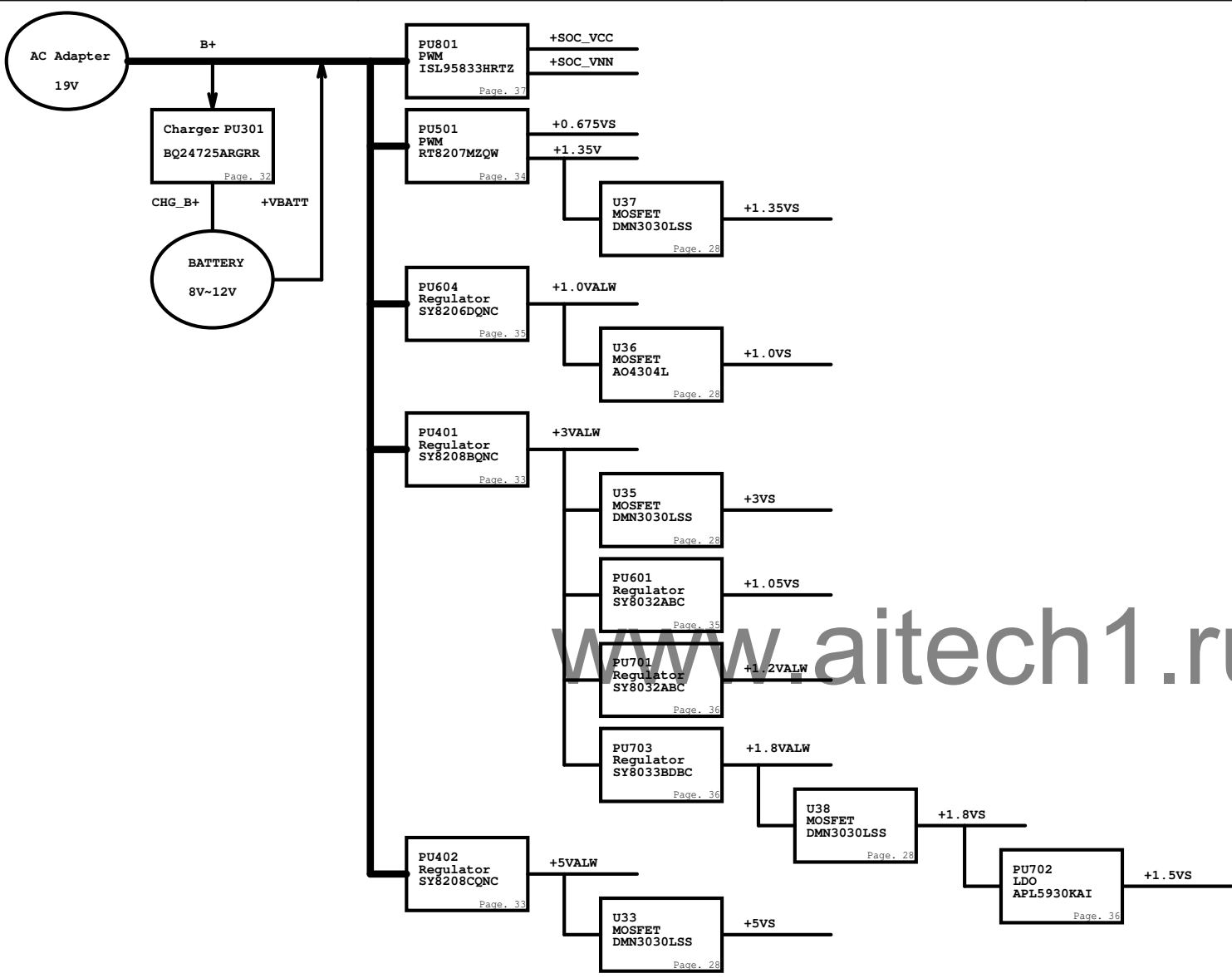


## NOTE:

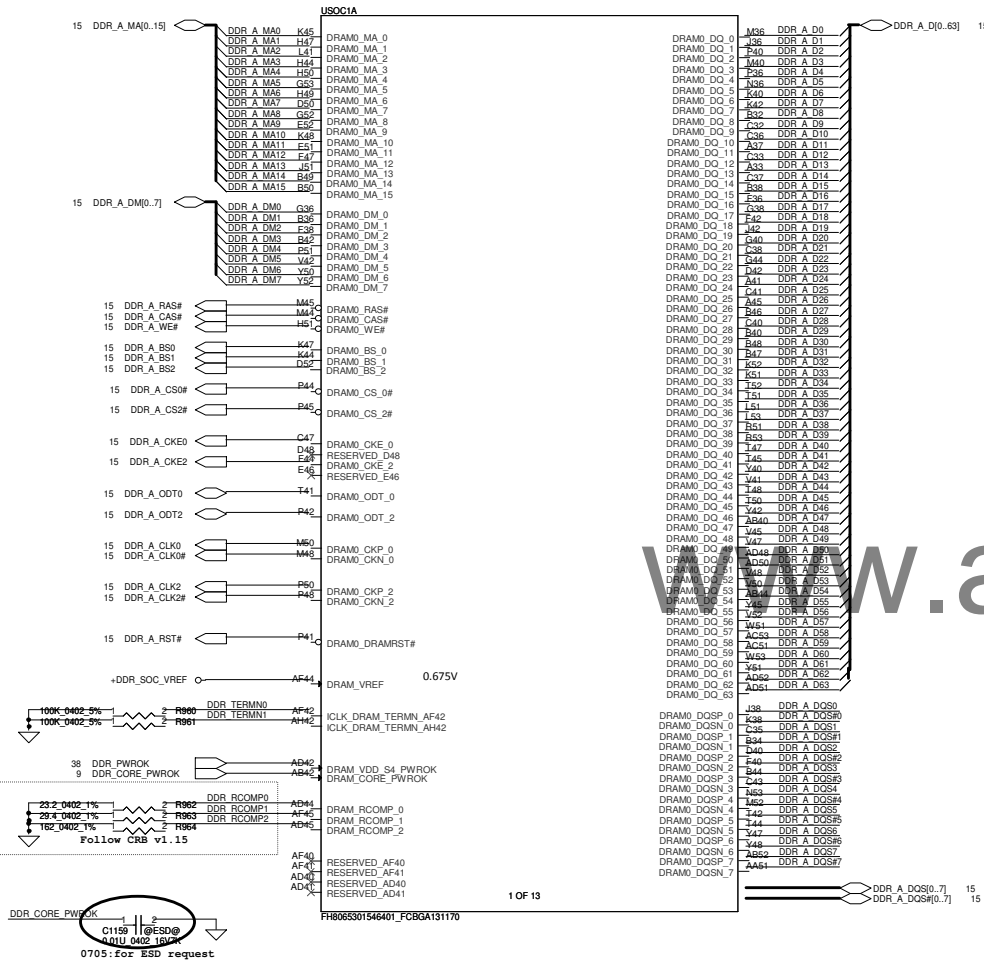
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

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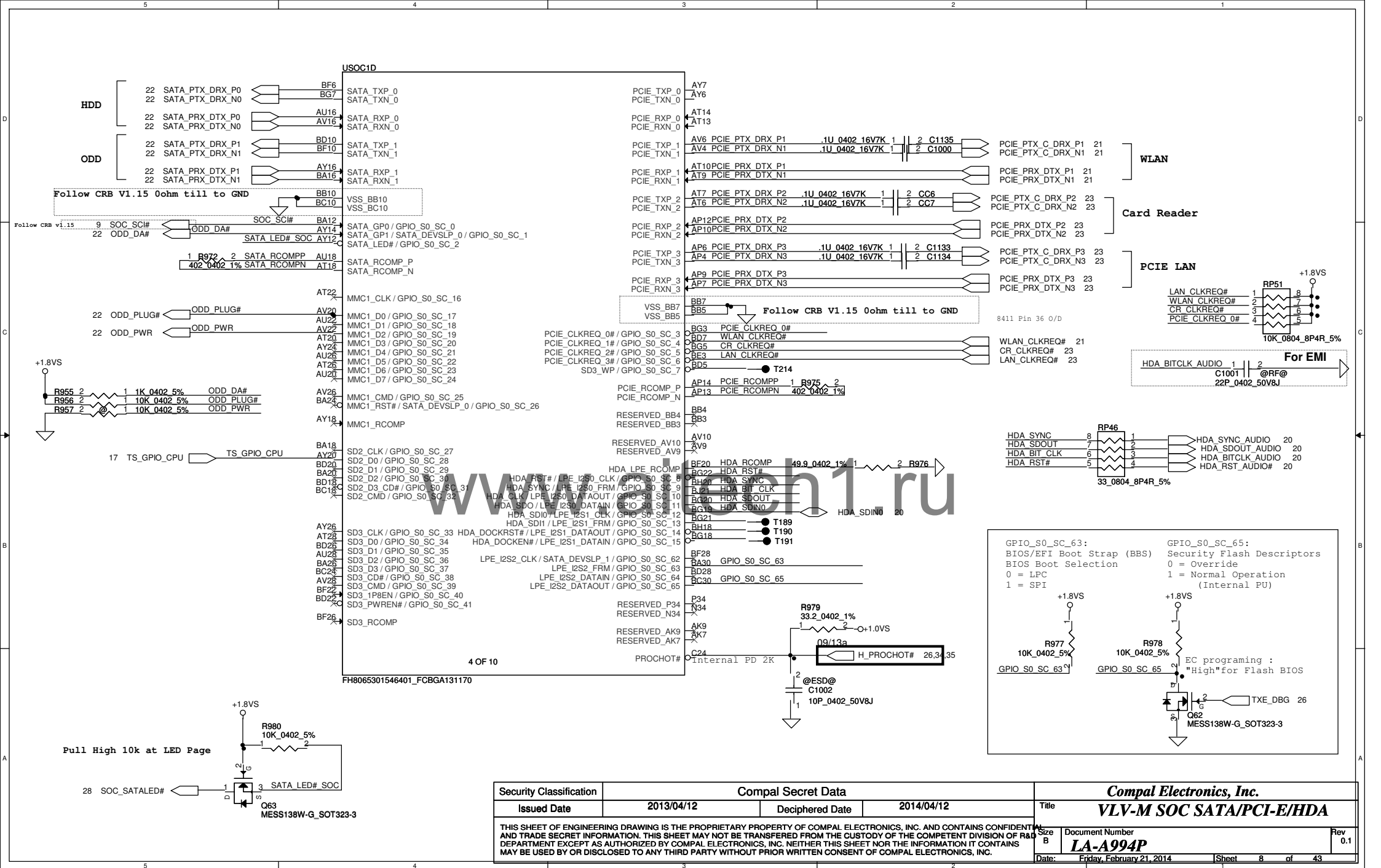


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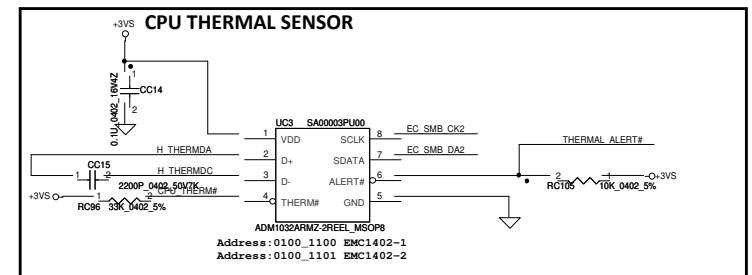
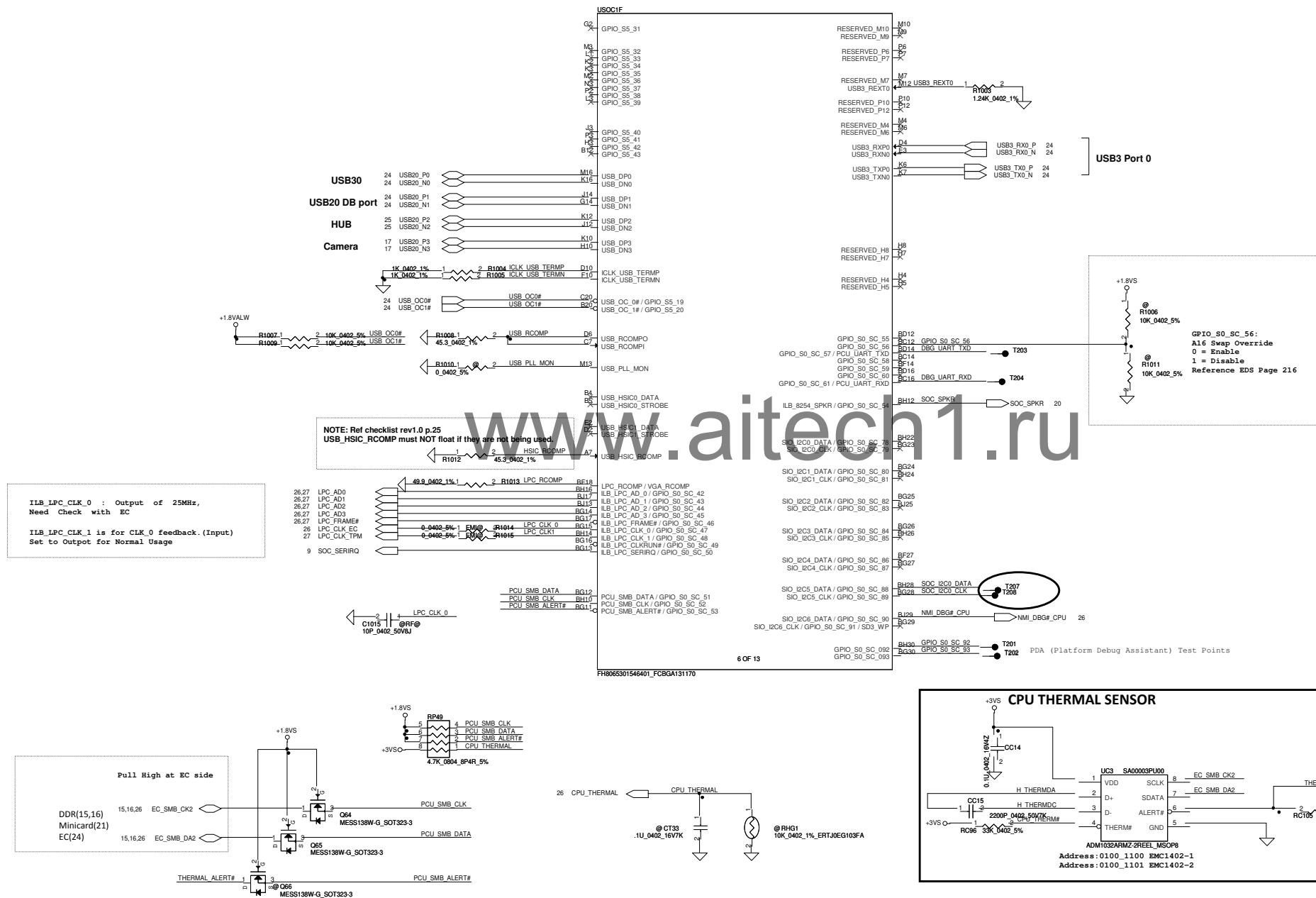
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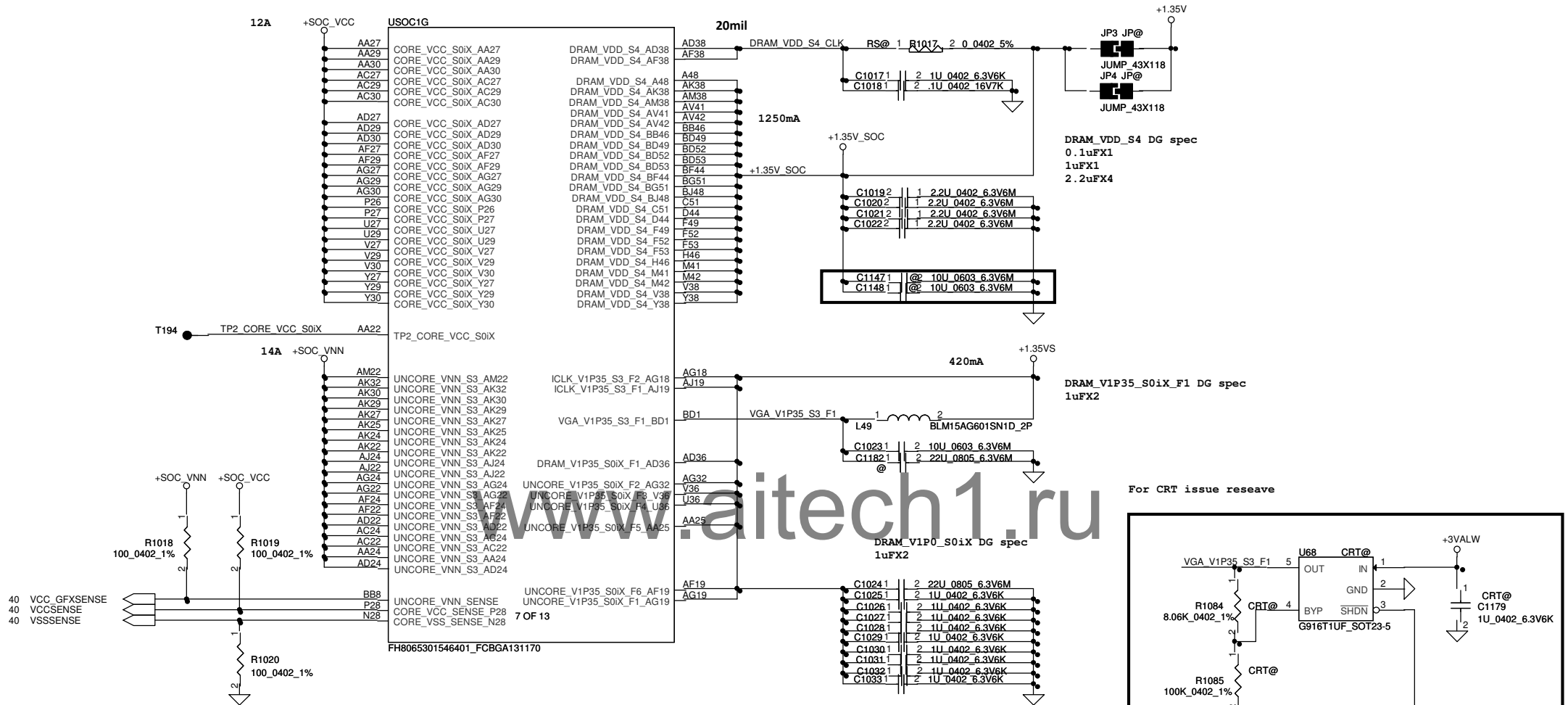




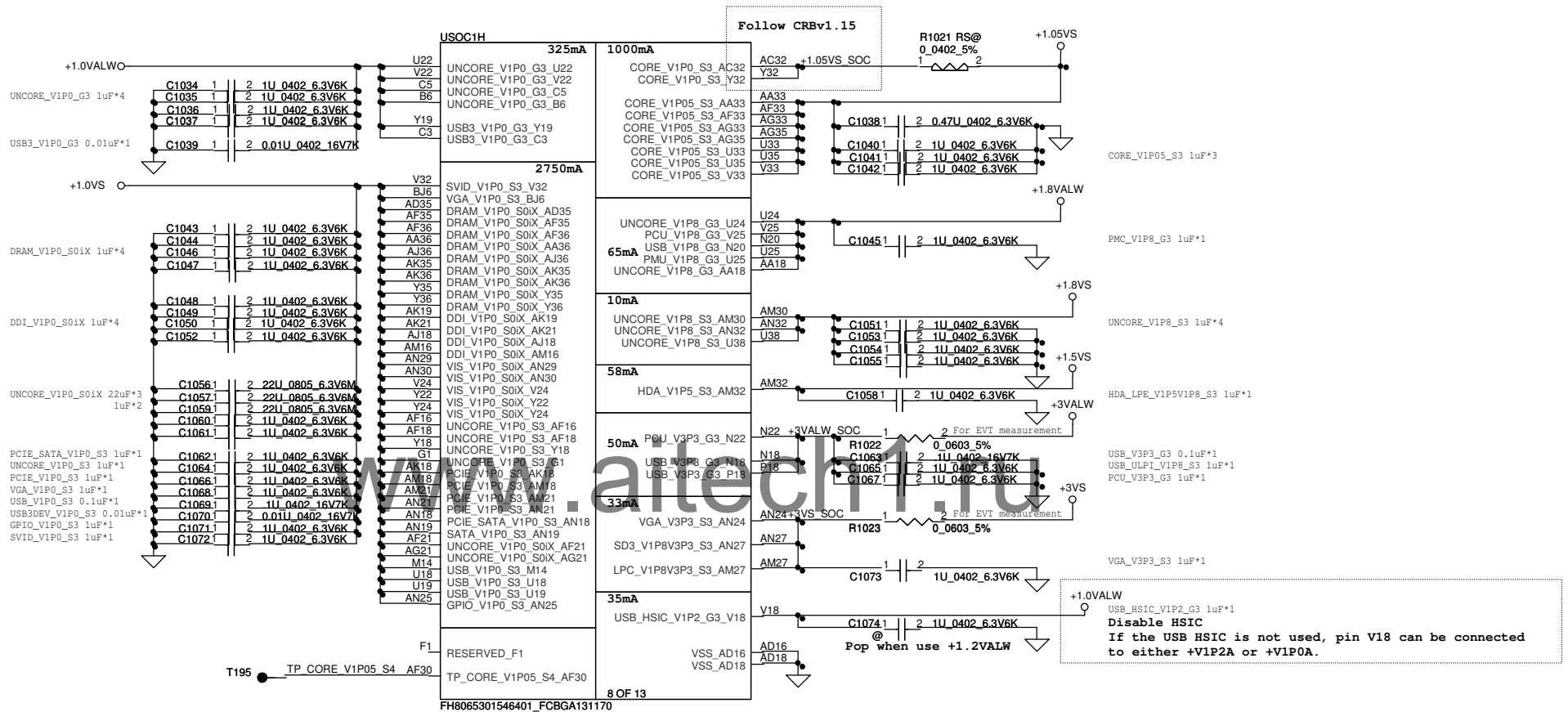




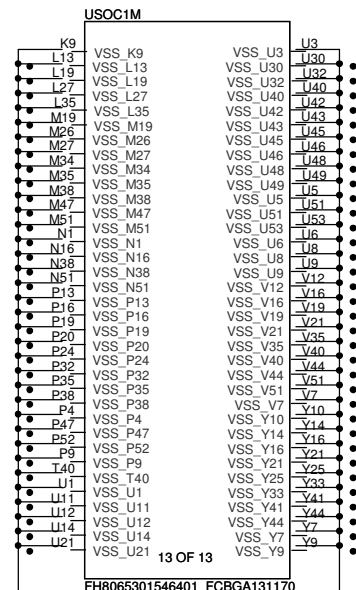
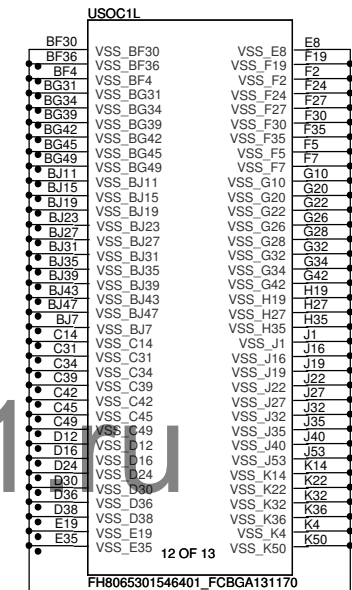
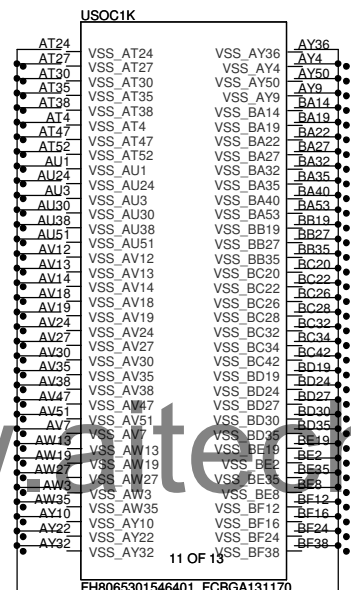
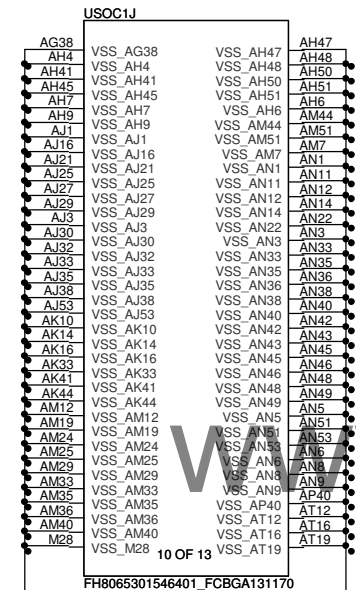
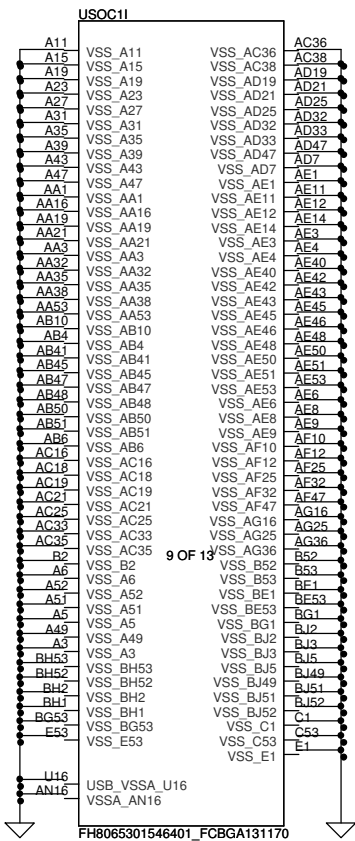
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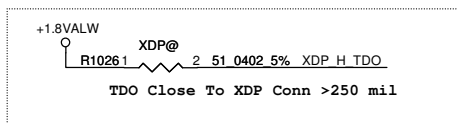
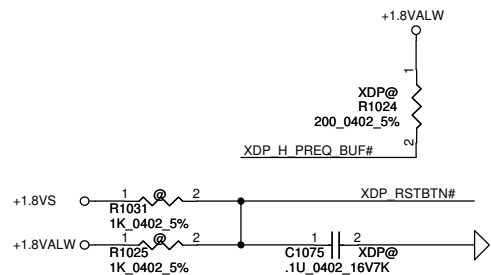
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## XDP-SFF-26Pin

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9 XDP\_H\_PREQ\_BUF# XDP H PREQ\_BUF#

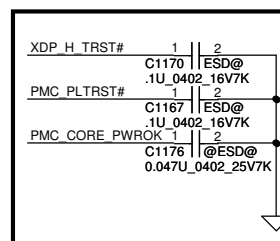
26,9 EC\_RSMRST# EC\_RSMRST#

26,9 PMC\_CORE\_PWROK PMC CORE PWROK

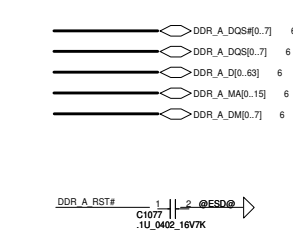
9 PMC\_PLTRST# PMC PLTRST#  
9 XDP\_RSTBTN# XDP\_RSTBTN#

9 XDP\_H\_TDO XDP H TDO  
9 XDP\_H\_TRST# XDP H TRST#

0927: for ESD request



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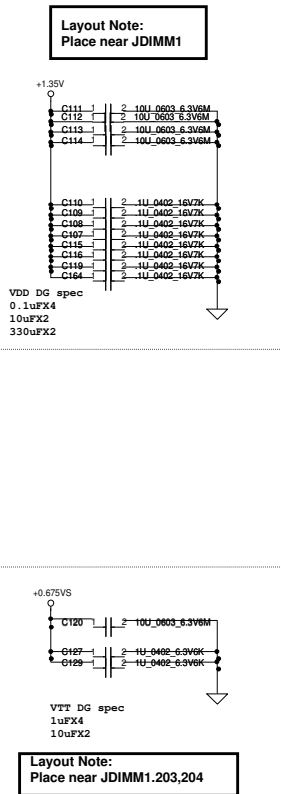
The image contains two circuit diagrams illustrating the placement of resistors for DDR\_A\_VREF\_DQ and DDR\_A\_VREF\_CA signals.

**Top Diagram (DDR\_A\_VREF\_DQ):**

- A 1.35V supply is connected to pin 1 of resistor R1027.
- Pin 2 of R1027 is connected to the signal line.
- Pin 1 of resistor R1028 is connected to the signal line.
- Pin 2 of R1028 is connected to ground.
- The signal line is connected to pin 1 of capacitor C1076.
- Pin 2 of C1076 is connected to ground.
- The signal line terminates at pin 1 of the DDR\_A\_VREF\_DQ pin.

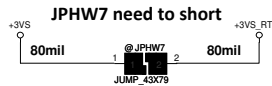
**Bottom Diagram (DDR\_A\_VREF\_CA):**

- A 1.35V supply is connected to pin 1 of resistor R1029.
- Pin 2 of R1029 is connected to the signal line.
- Pin 1 of resistor R1030 is connected to the signal line.
- Pin 2 of R1030 is connected to ground.
- The signal line is connected to pin 1 of capacitor C1078.
- Pin 2 of C1078 is connected to ground.
- The signal line terminates at pin 1 of the DDR\_A\_VREF\_CA pin.

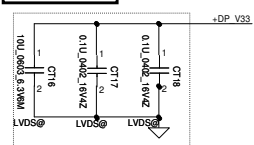


**<Address: SA1:SA0=00 (A0H)>**  
**DIMM\_1 STD H:4mm**

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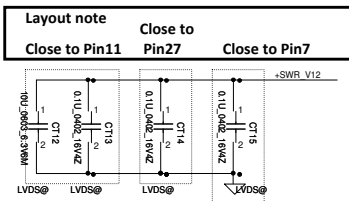
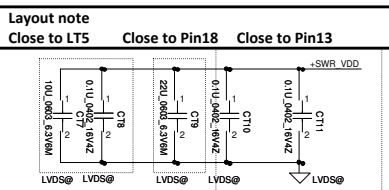
**Layout note**  
Close to Pin3



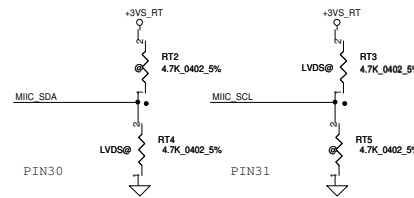
## SWR / LDO Mode select

	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

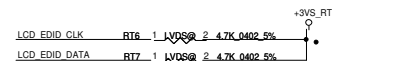
\* If use 2132R, please select LDO mode as default.



\*ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.  
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.  
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.  
( \*Default mode )



<CONN>



<CONN>  
<CPU>

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

\* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

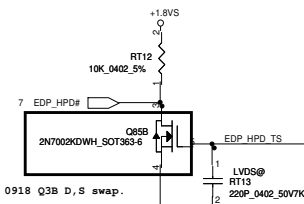
	PIN16	Accept voltage input (high level)
2132S	3.3V	
2132R	1.5~3.3V	

\* Version R has internal level shifter, remove level shifter circuit on AMD platform

## Different between 2132S and 2132R

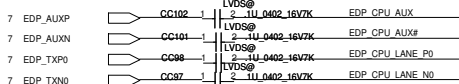
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

<CPU 1.8V level>

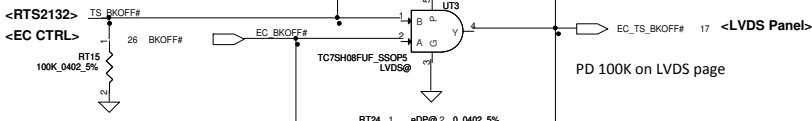


**Layout note**  
Close to Pin8

<CPU>



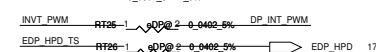
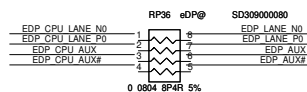
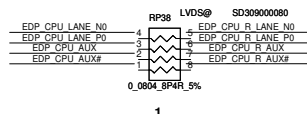
<SI> Update UT3 footprint (As UV11) 10/09



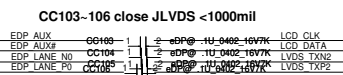
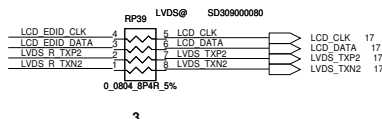
131111 add RT15 for power sequence

<LVDS panel> ==>

<eDP panel> ==>



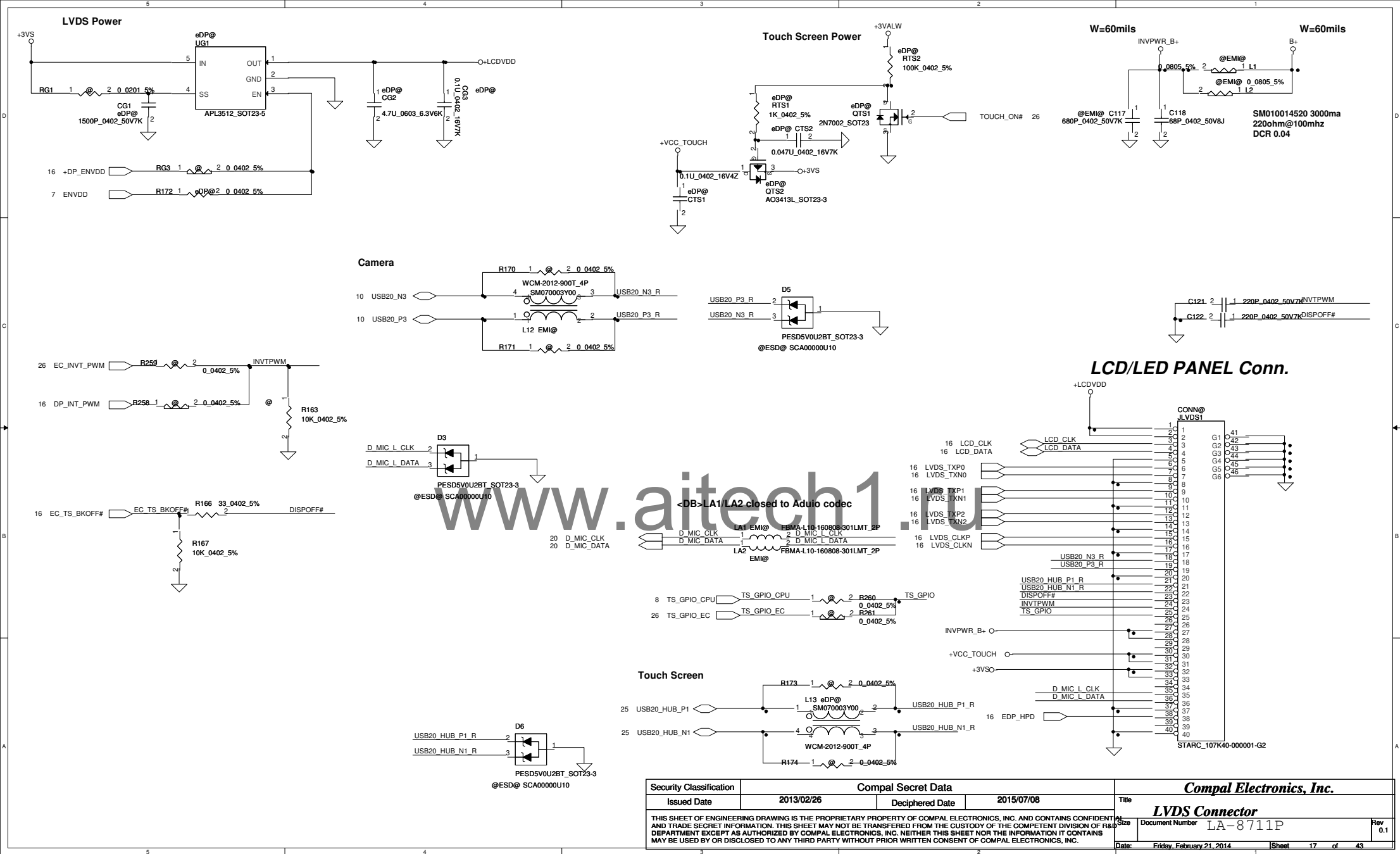
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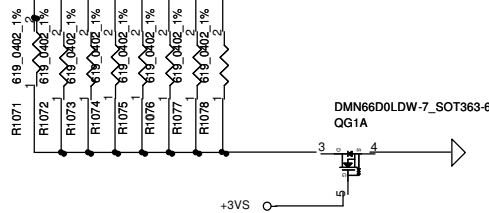
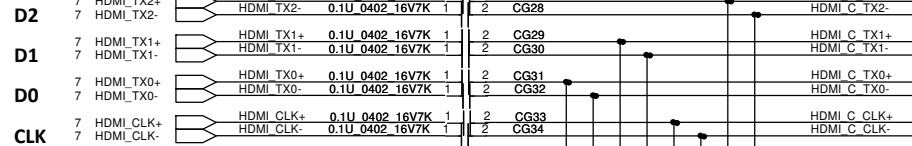
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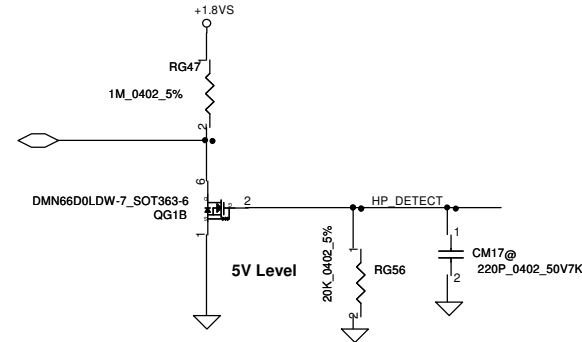




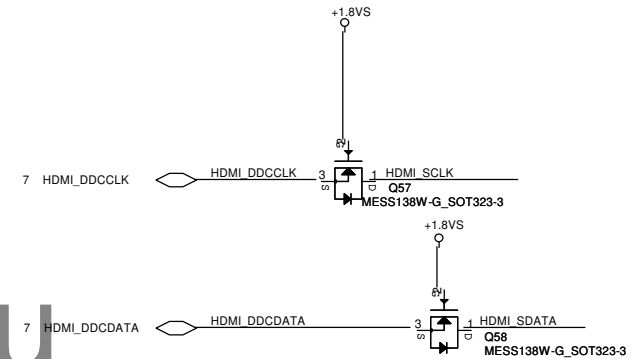
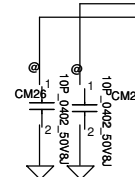
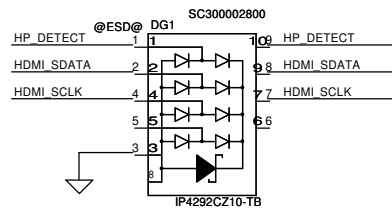
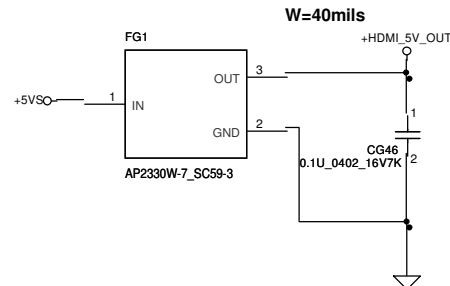
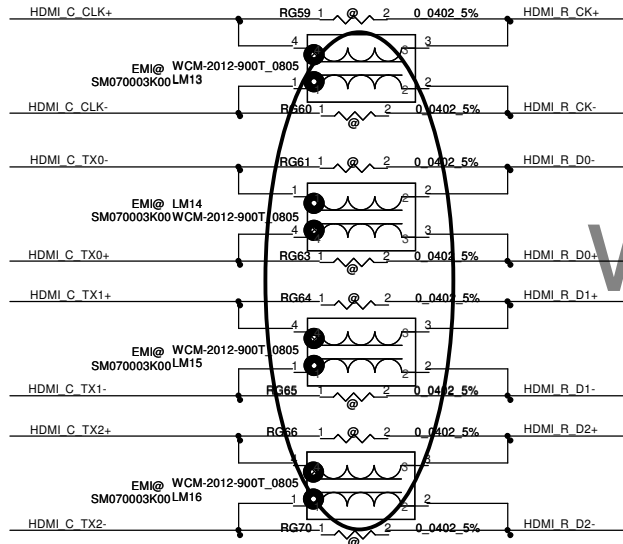
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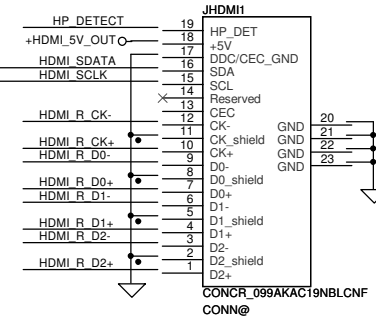
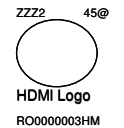
7 HDMI\_HPD#



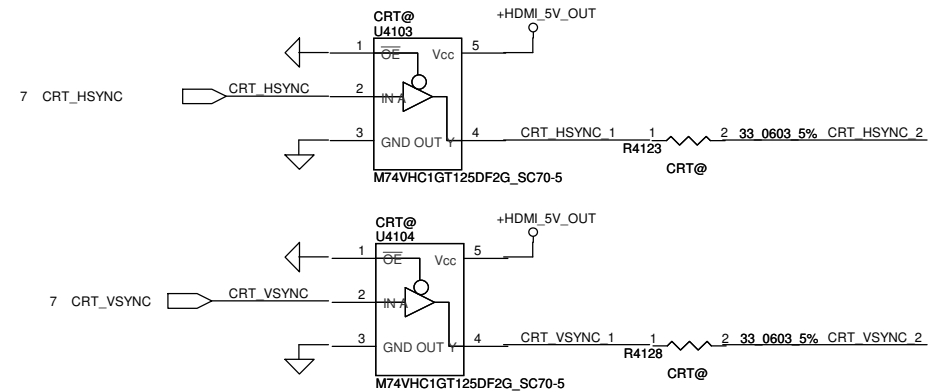
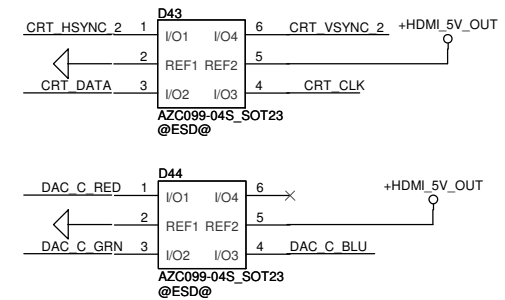
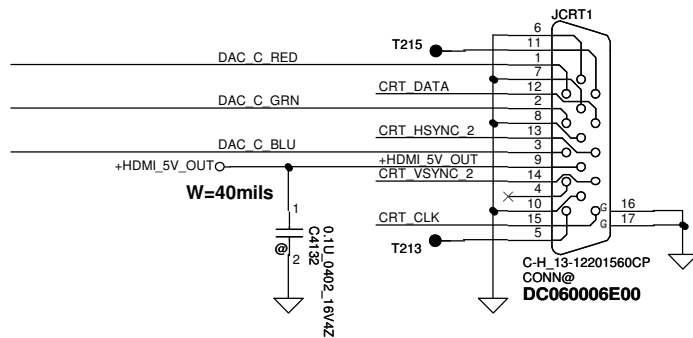
10/21 BOM change SM070003K00



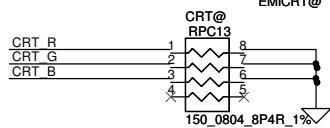
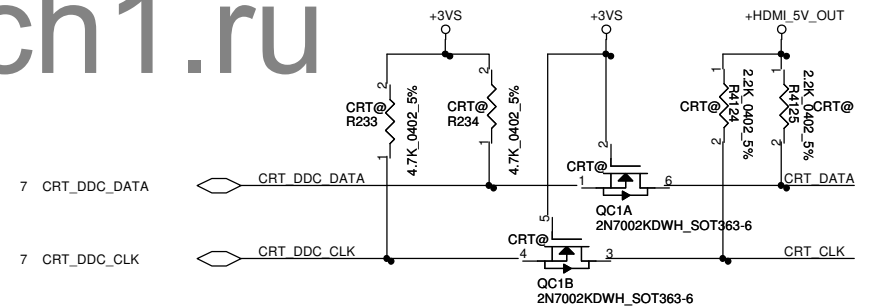
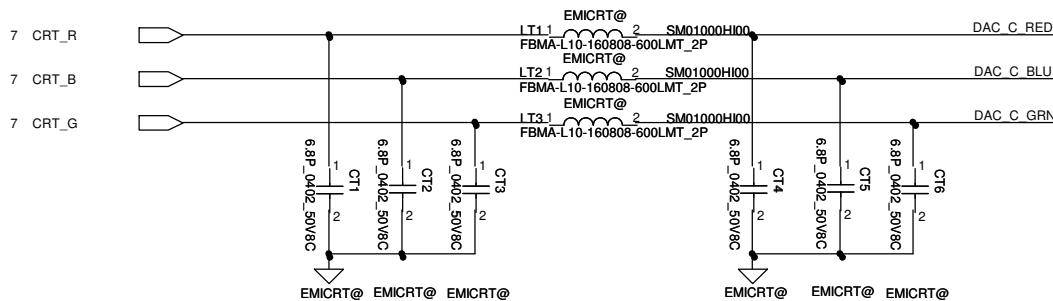
HDMI Conn.



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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	HDMI Conn/Level shift
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				LA-A992P	Rev 0.1
				Date:	Friday, February 21, 2014
				Sheet	18 of 43

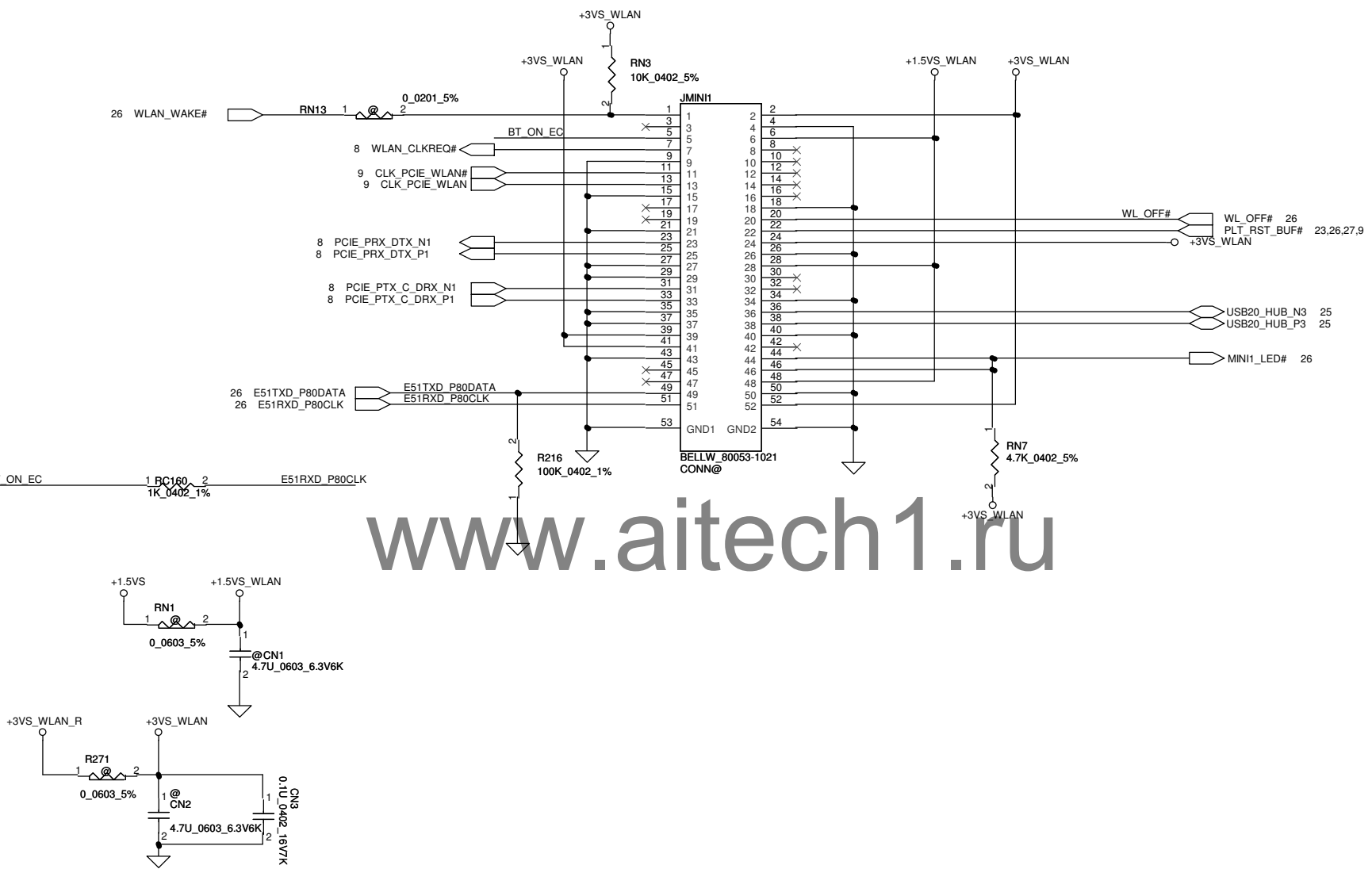


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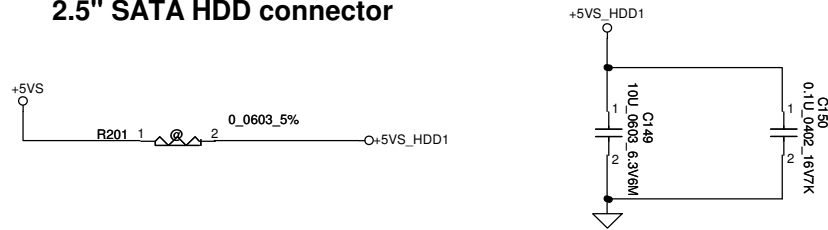
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
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				LA-A994P	0.1
Date: Friday, February 21, 2014				Sheet	19 of 43



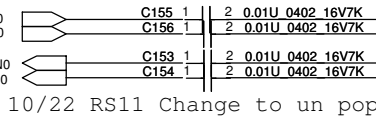


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	WLAN
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				LA-A992P	Rev 0.1
				Date:	Friday, February 21, 2014
				Sheet	21 of 43

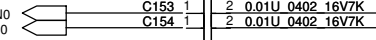
## 2.5" SATA HDD connector



8 SATA\_PTX\_DRX\_P0  
8 SATA\_PTX\_DRX\_N0

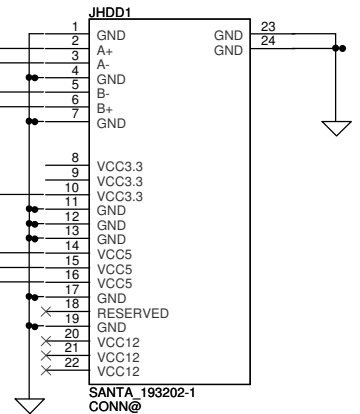


8 SATA\_PRX\_DTX\_N0  
8 SATA\_PRX\_DTX\_P0

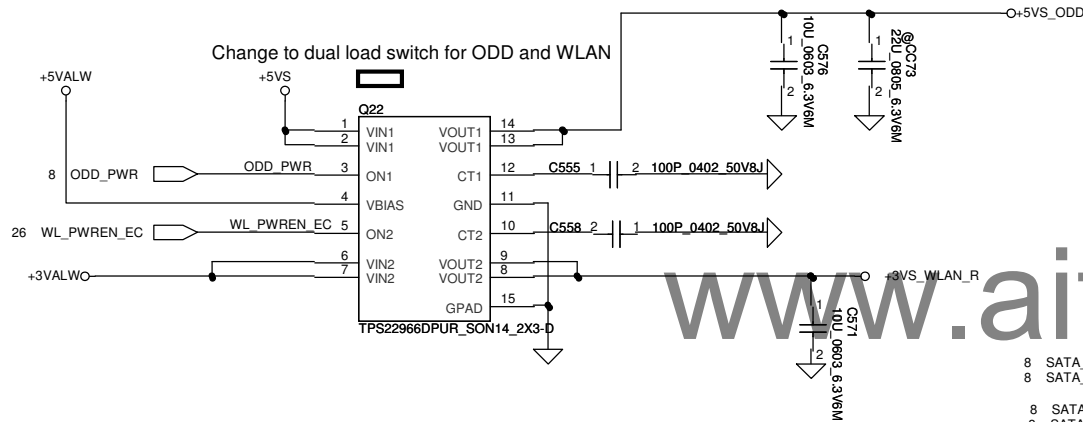


+3VS RS11 1 2 0.0402 5% JHDD P10

+5VS\_HDD1C

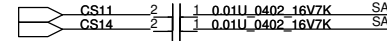


Change to dual load switch for ODD and WLAN

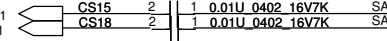


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8 SATA\_PTX\_DRX\_P1  
8 SATA\_PTX\_DRX\_N1

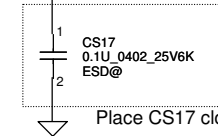
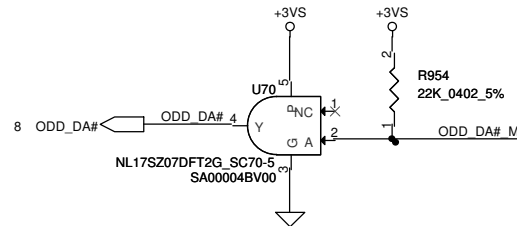


8 SATA\_PRX\_DTX\_N1  
8 SATA\_PRX\_DTX\_P1



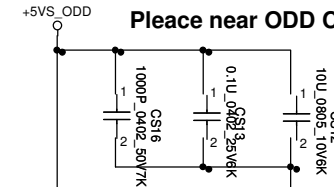
8 ODD\_PLUG#

ODD DA# M

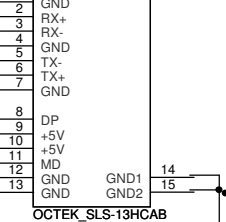


Place CS17 close to JODD

Place near ODD Connector

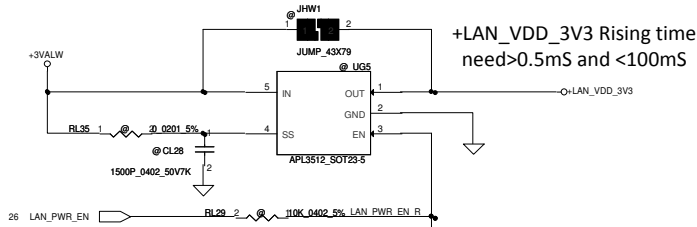


JODD1

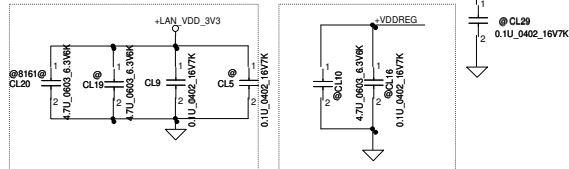


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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	ODD/SATA Conn
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				Date:	Friday, February 21, 2014
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## JHW1 need to short

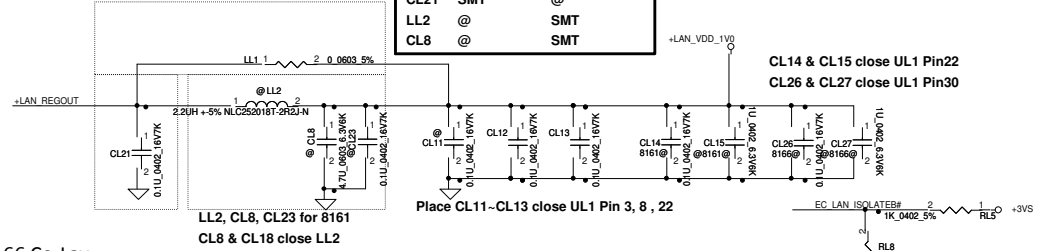


+LAN\_VDD\_3V3 Rising time need>0.5ms and <100ms



CL9 & CL5 close to UL1: Pin 11,32  
CL19 close to UL1: Pin 32  
CL20 close to UL1: Pin 11  
CL10 & CL16 close to UL1: Pin 23

## RTL8151G (LDO mode)



	LDO mode	Switching mode
LL1	SMT	@
CL21	SMT	@
LL2	@	SMT
CL8	@	SMT

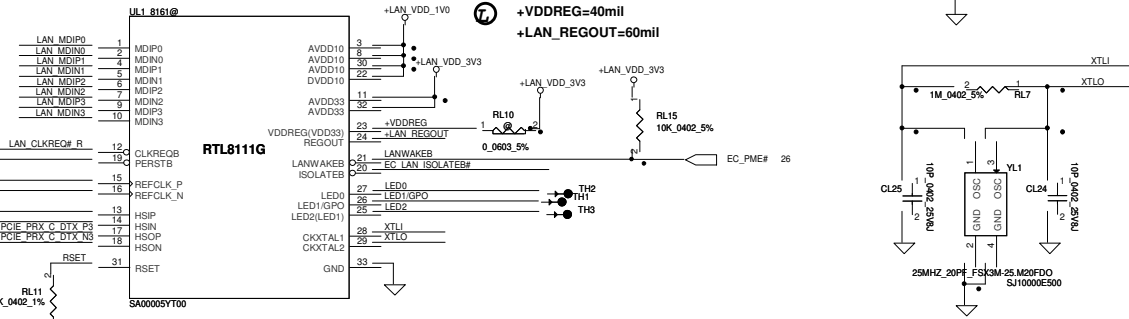
CL14 & CL15 close UL1 Pin22  
CL26 & CL27 close UL1 Pin30

Place CL11-CL13 close UL1 Pin 3, 8, 22

LL2, CL8, CL23 for 8161

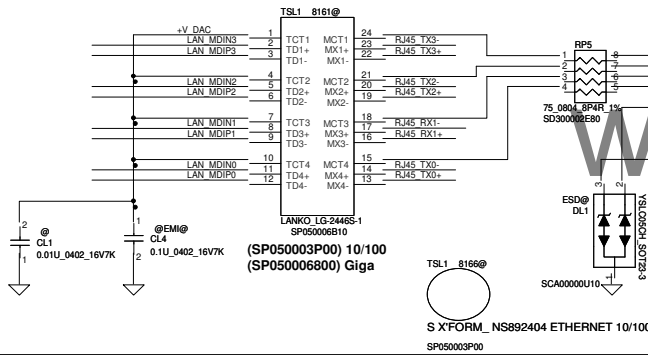
CL8 & CL18 close LL2

## 8151/8166 Co-Lay



+LAN\_VDD\_3V3=40mil  
+VDDREG=40mil  
+LAN\_REGOUT=60mil

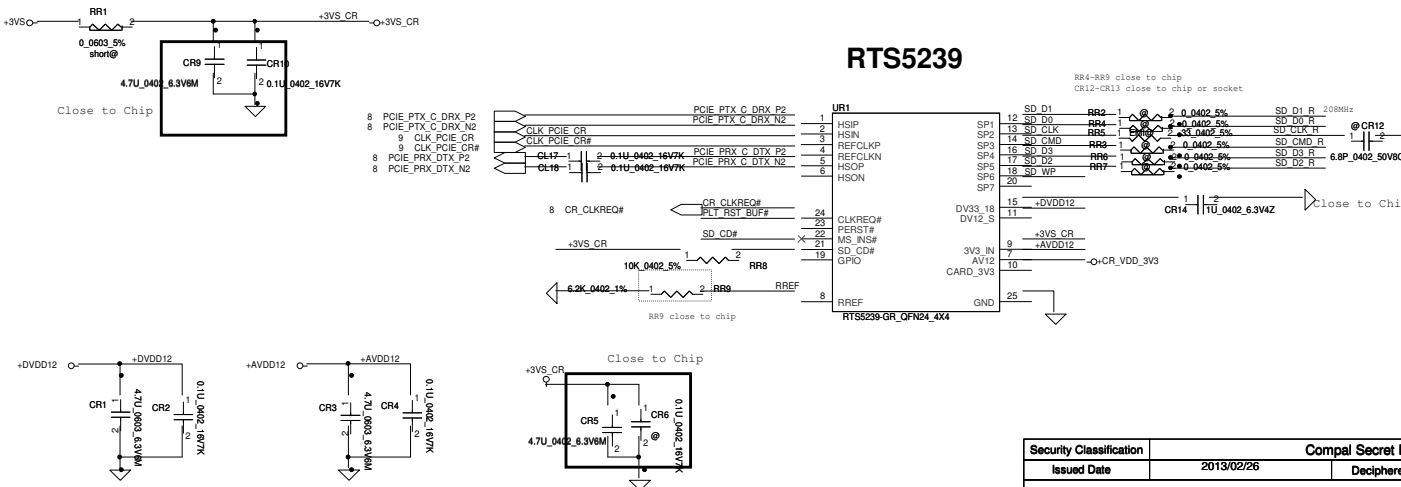
## SP050005L00 Footprint



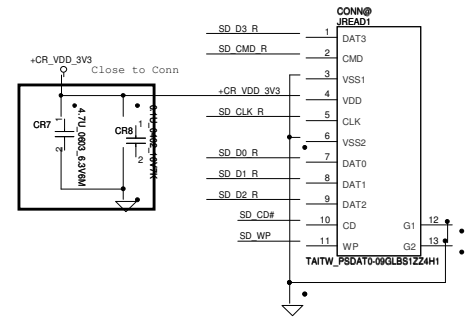
(SP050003P00) 10/100  
(SP050006800) Giga

S X'FORM\_NS892404 ETHERNET 10/100  
SP050003P00

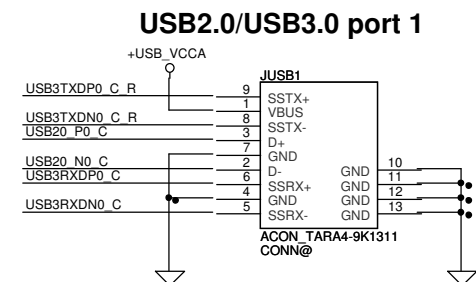
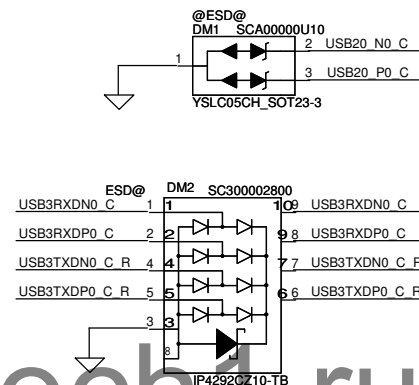
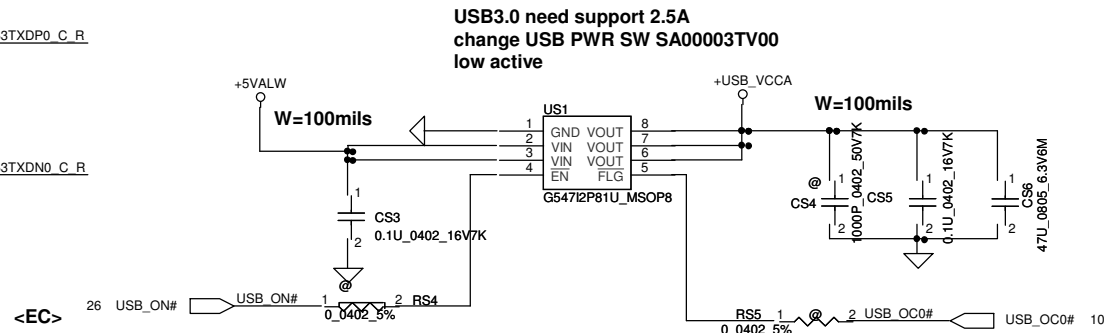
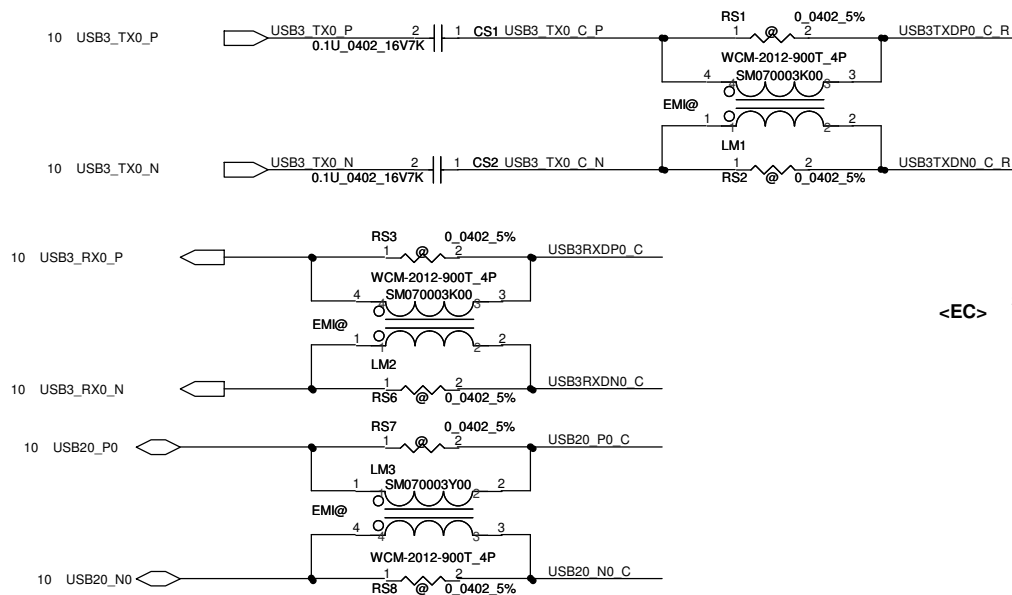
## RTS5239



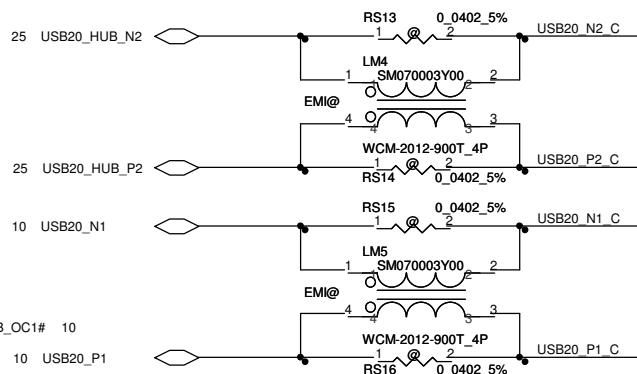
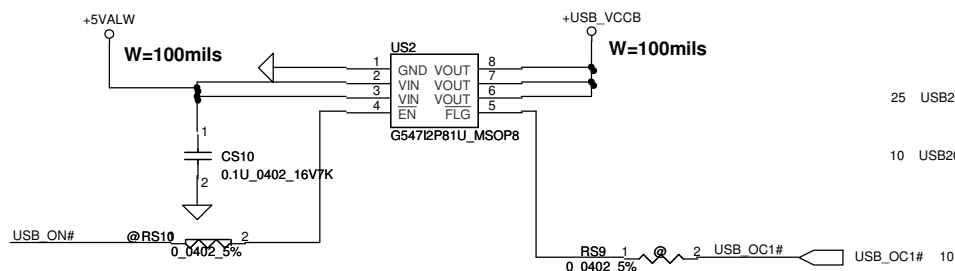
## Card Reader Connector



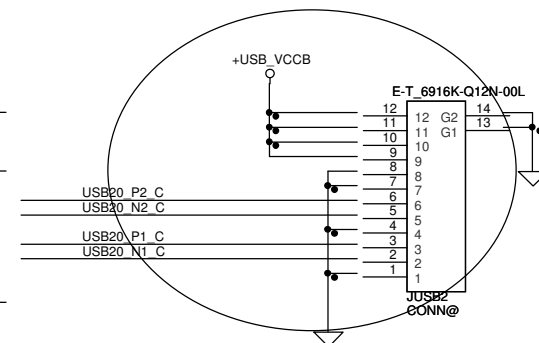
Security Classification	Compal Secret Data	Title	LAN 8111G
Issued Date	2013/02/26	Deciphered Date	2015/07/08
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## USB2.0 port x 2

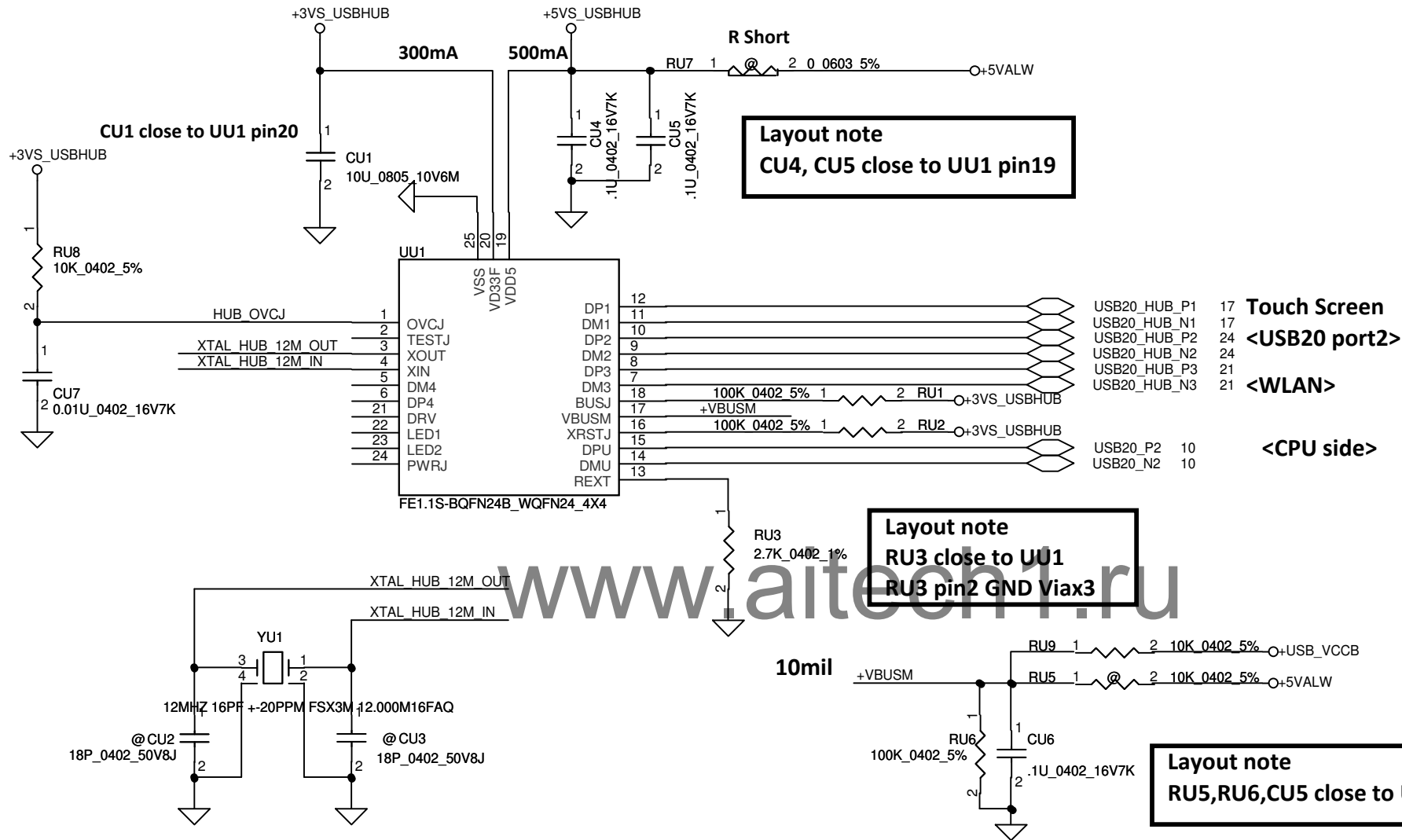


## 131109 Follow 15" Haswell LA-A992PR02



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	USB 3.0/2.0 conn
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				Date: Friday, February 21, 2014	Sheet 24 of 43

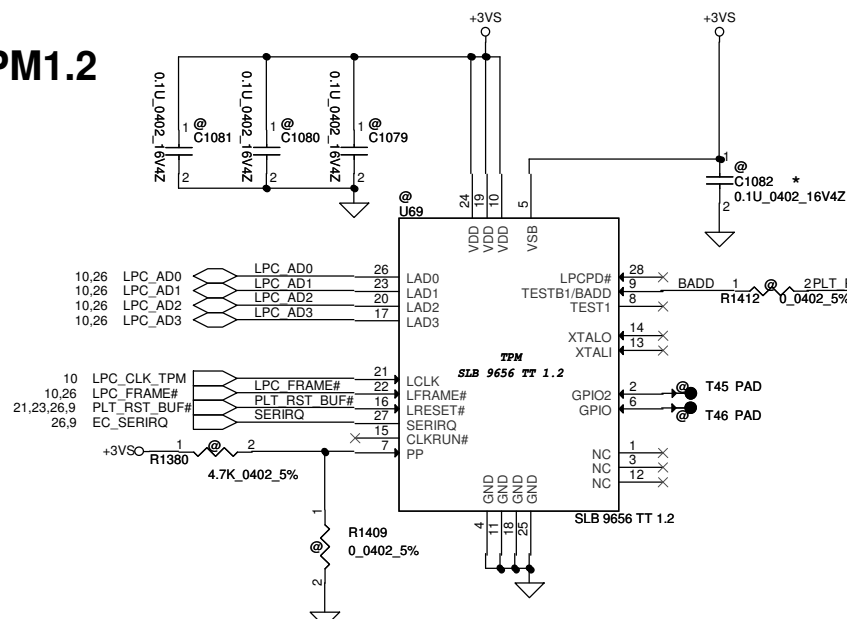




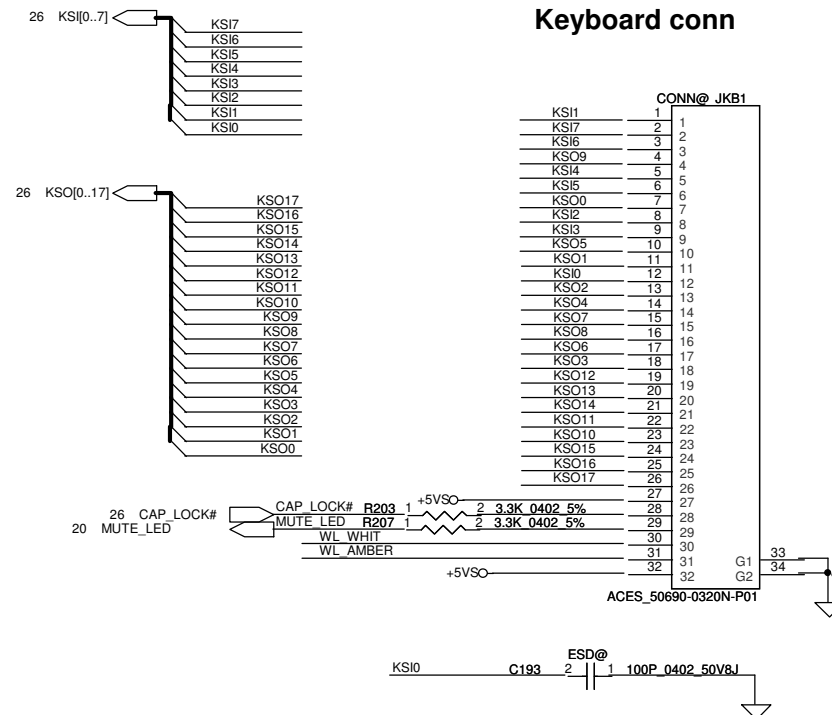
Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2013/02/26		Deciphered Date		2015/07/08		Title		
		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				USB2.0 Hub				
						Size	Document Number		Rev	
						Custom	LA-A994P		0.1	
		Date: Friday, February 21, 2014		Sheet 25 of 43						



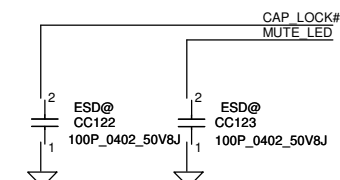
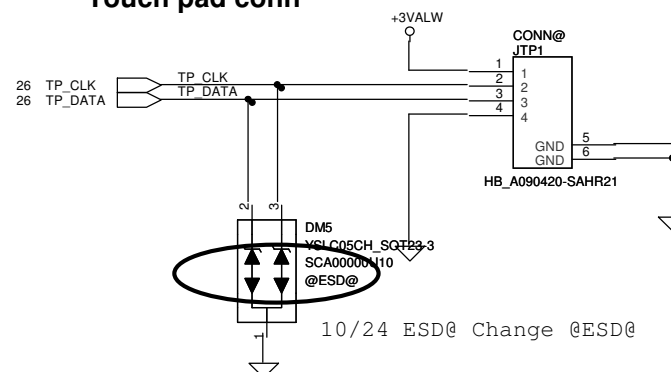
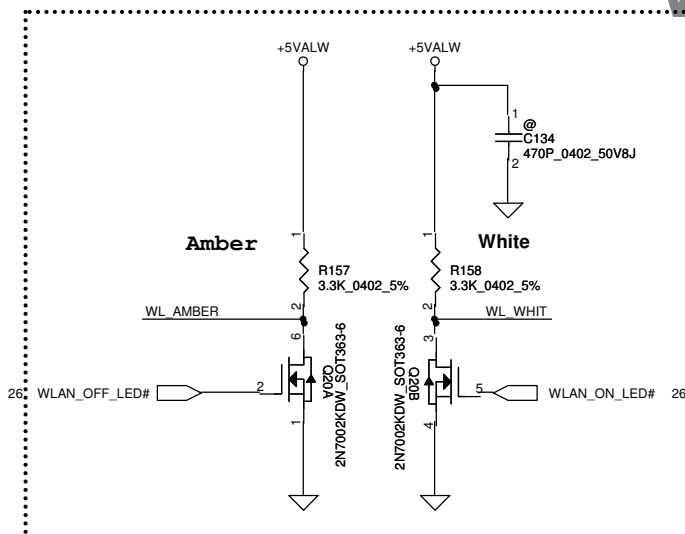
## TPM1.2



## Keyboard conn

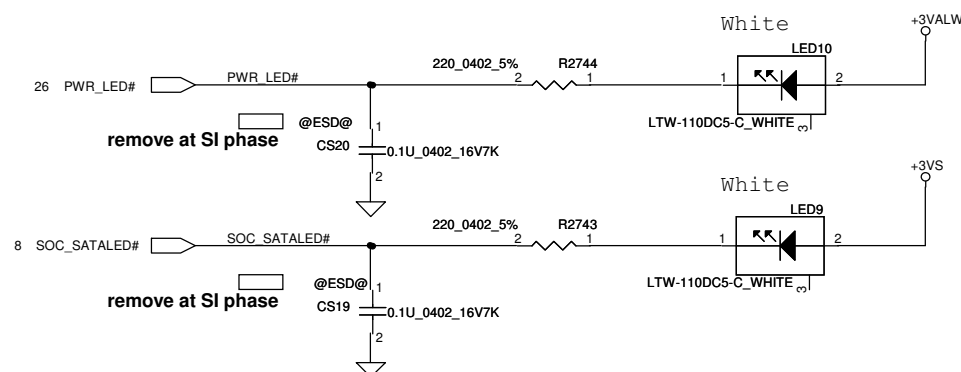
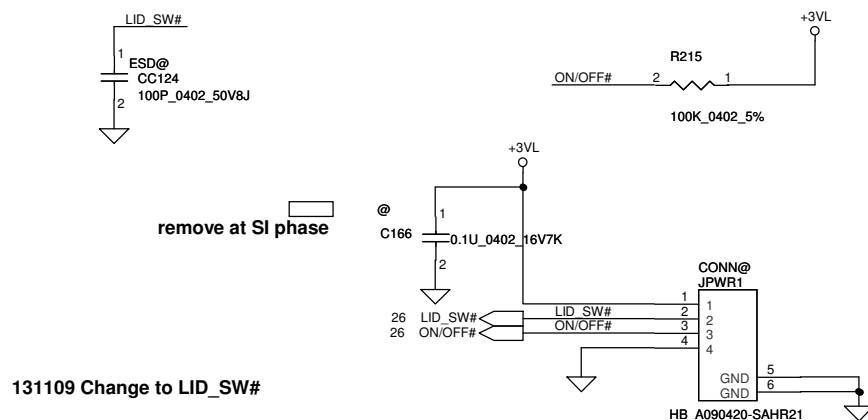


## Touch pad conn

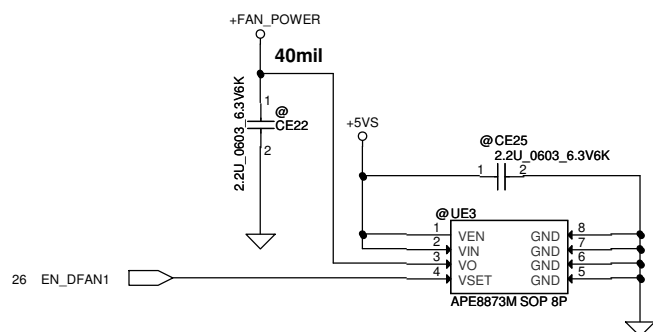


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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	KB/TP	
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				LA-A992P		
				Date: Friday, February 21, 2014	Sheet	27 of 43

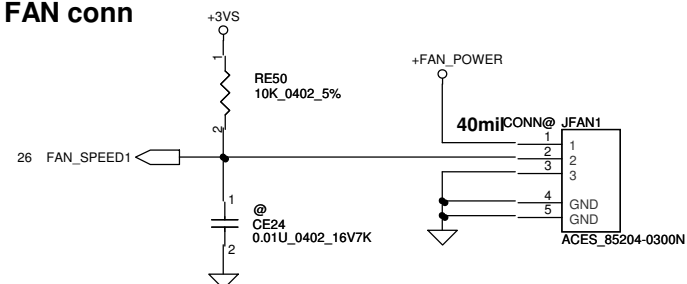
# Power Button Connector



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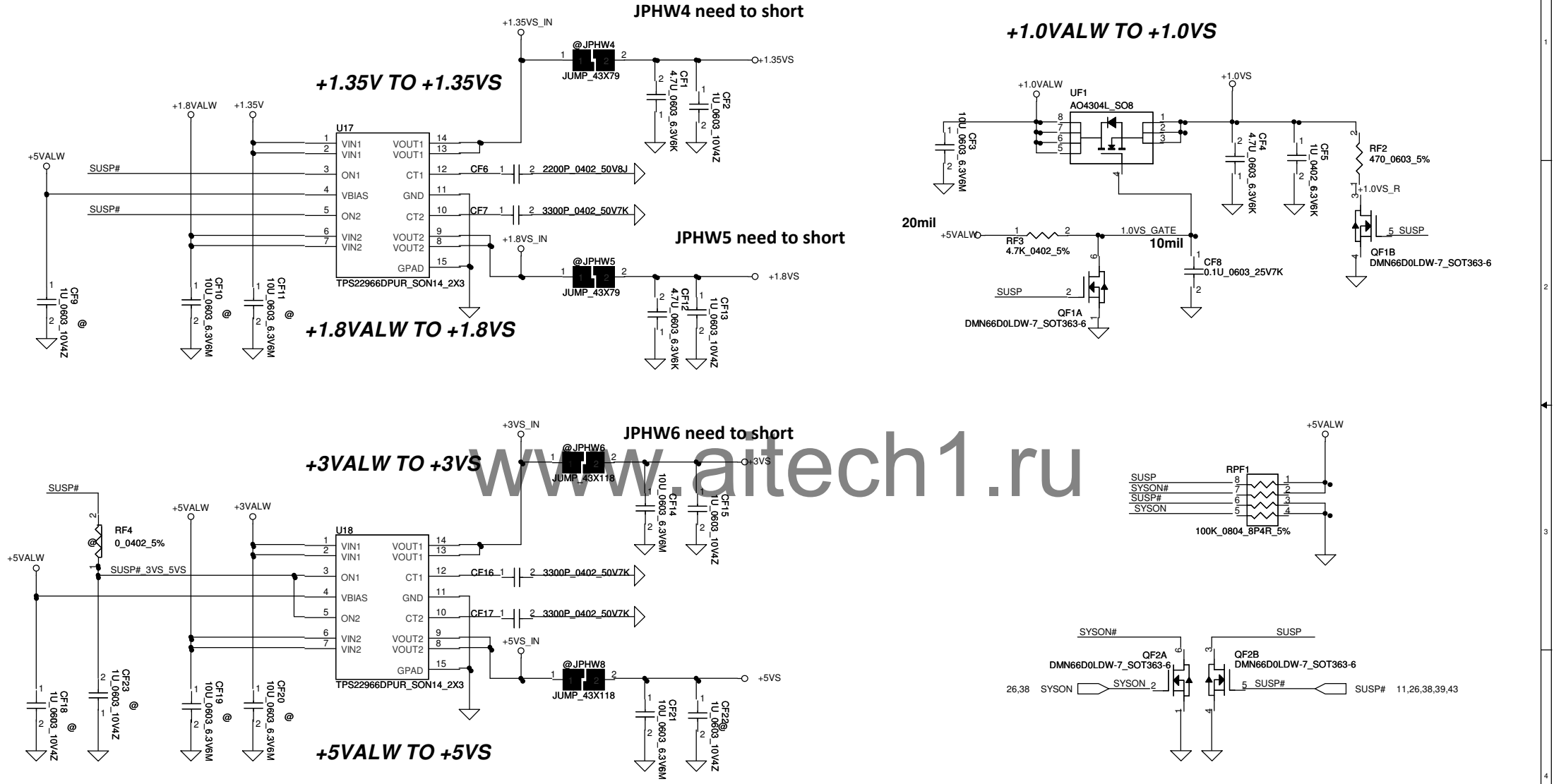


## FAN conn



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			PWRBTN/FAN	
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				0.1
Date: Friday, March 14, 2014		Sheet 28 of 43		

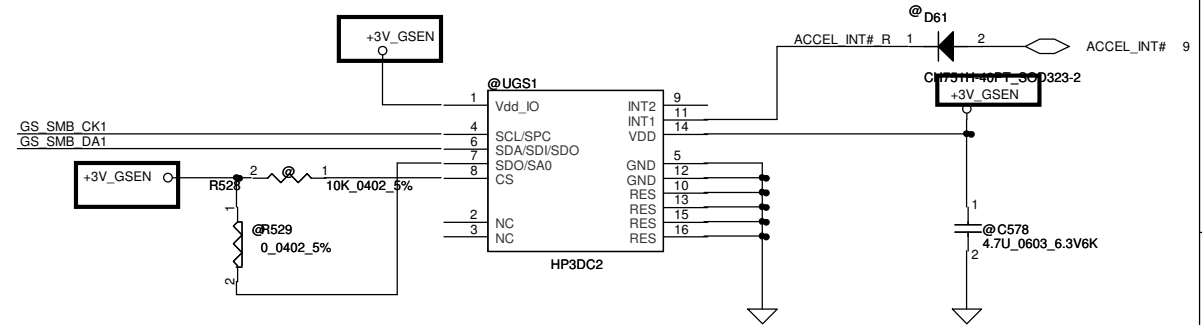
# Bay trail M new power up sequence



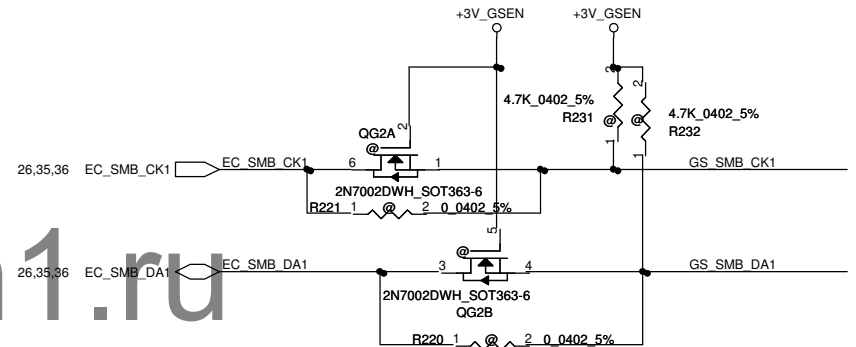
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	DC Interface
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				Date:	Friday, February 21, 2014
				Sheet	29 of 43

10/21 +3VALW Change +3VL

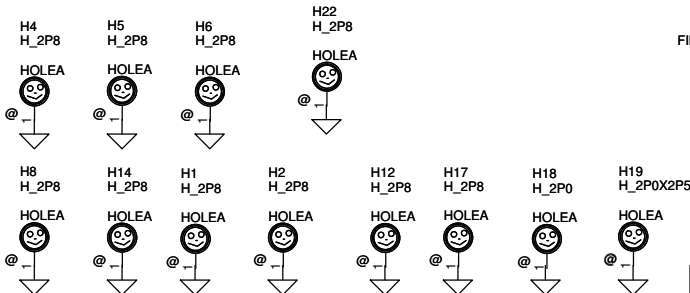
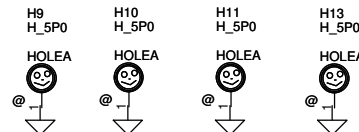
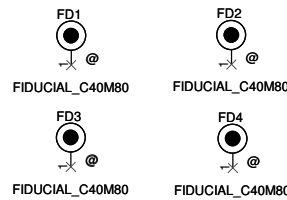
# ACCELEROMETER



Must be placed in the center of the system.

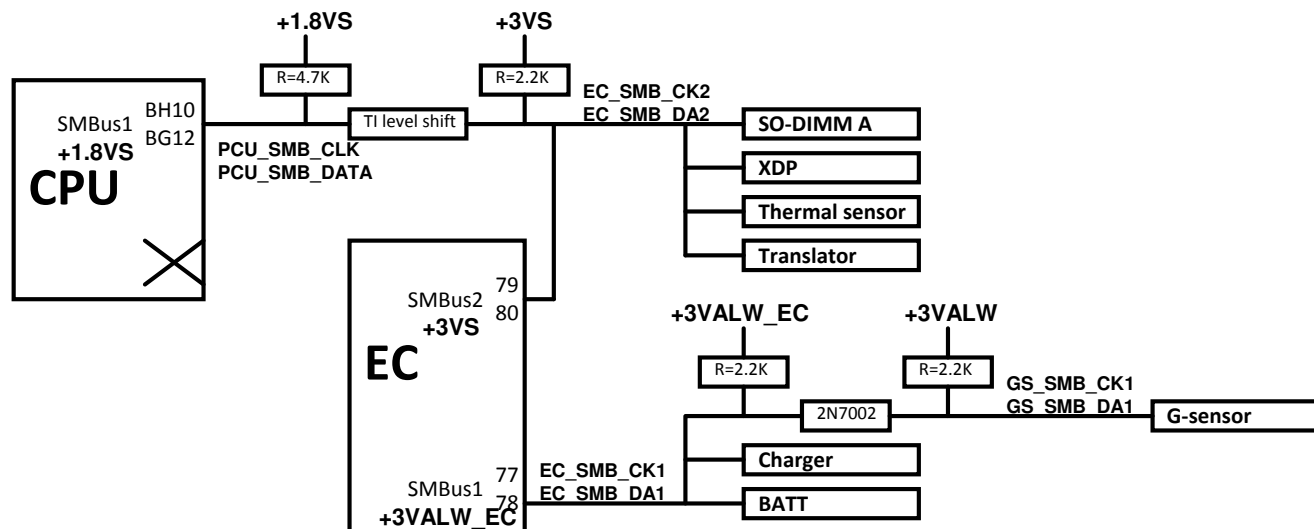


Reserve MOS for power leakage



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	LED/Screw hole
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## <SMBus Routing>



<USB2.0/3.0 port>

USB2.0	USB3.0	Function	Note
0	<b>X</b>	Left port (USB2.0)	
1	0	Right port-1 (USB2.0/3.0)	
2	<b>X</b>	Right port-2 (USB2.0)	
3	<b>X</b>	WLAN	USB2.0x4 Hub
4	<b>X</b>	Touch screen	USB2.0x4 Hub
5	<b>X</b>	Camera	USB2.0x4 Hub
6	<b>X</b>	NC	USB2.0x4 Hub

<PCI-E port>

PCI-E	Function	Note
0	LAN	
1	WLAN	
2	Card reader	
3	NC	

<SATA port>

PCI-E	Function	Note
0	HDD	
1	NC	

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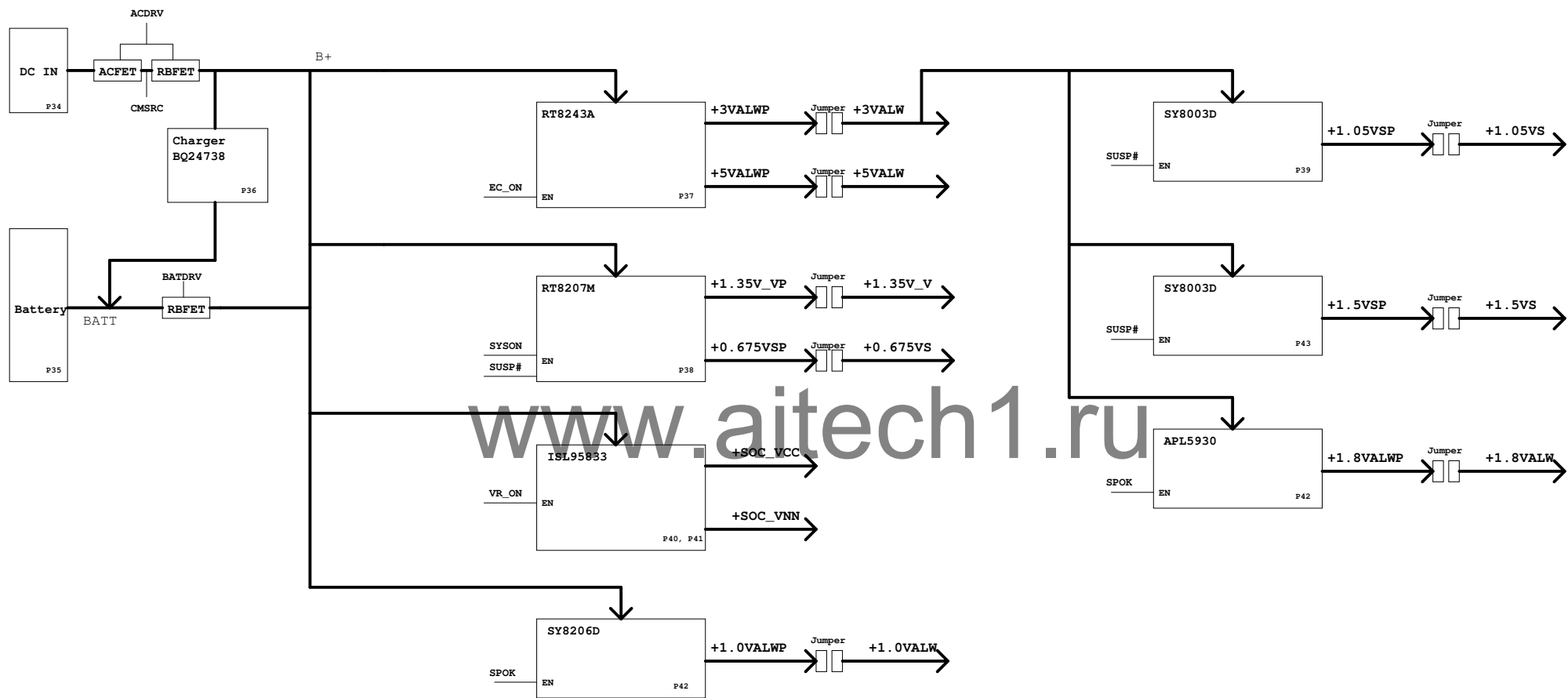
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29		131107		1.Change PN of RPF1 from SD302100380 to SD309100380		
2	28		131109		1.Change Control pin of LID from NEW_LID_SW(R218) to LID_SW#(R219)		
3	24		131109		1.Follow 14" Haswell LA-A993PRO2's USB2 Conn.		
4	16		131111		1.Update UT3 footprint follow Haswell platform		
5	22		131111		1.Delete R954 ,Q84 for ODD_DA# 2.unpop RS11		
6	18		131111		1.Change PN of LM13,LM14,LM15 & LM16 from SM070001V00 to SM070003K00		
7	30		131111		1.Change Power Rail of G sensor from +3VALW to +3VL & unpop QG2		
8	30		131111		1.pop DM5		
9	26		131111		1.change Board ID to SI phase		
10	16		131111		1.add PD 100K RT15K for power sequence		

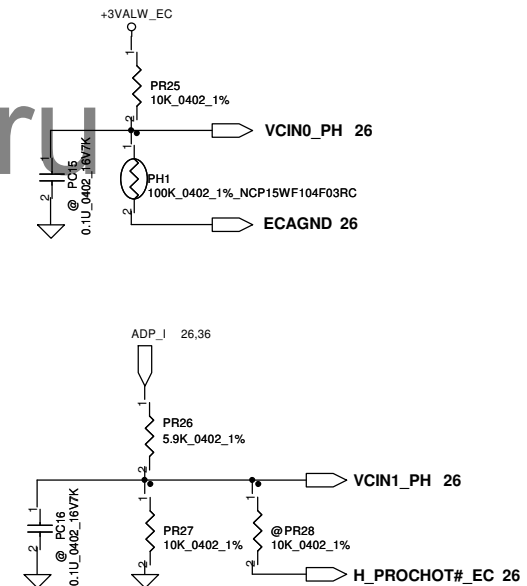
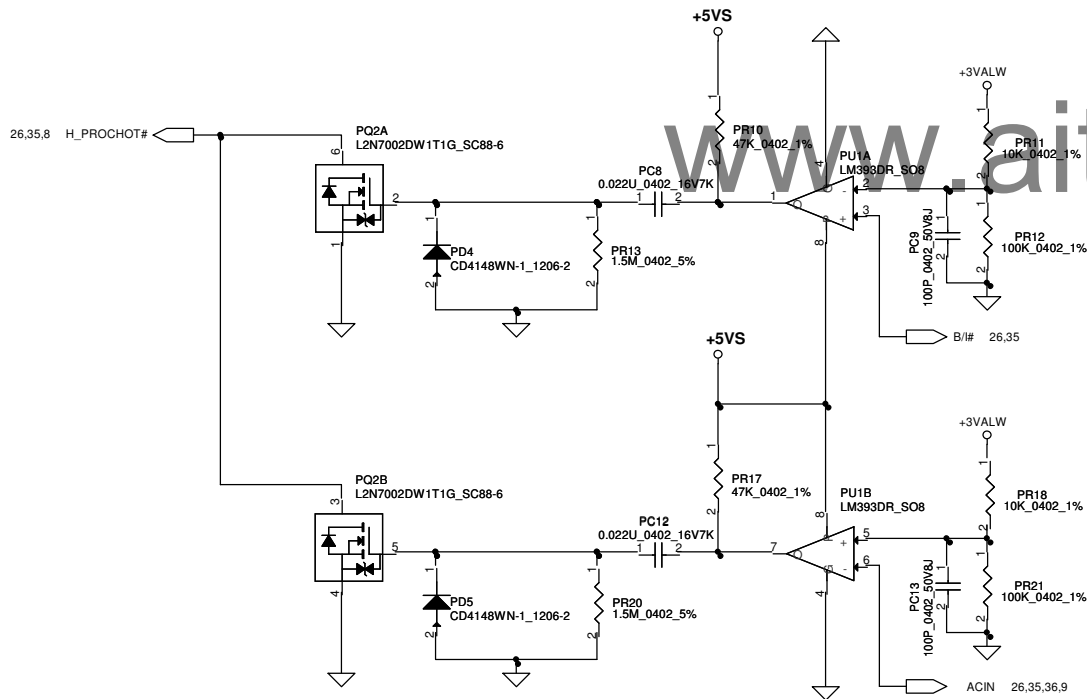
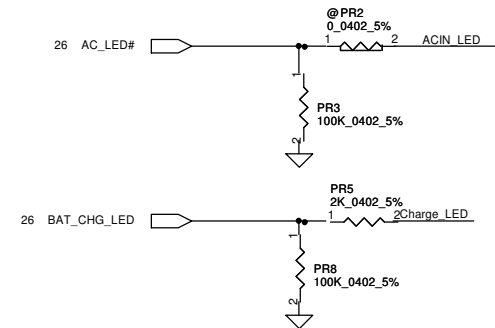
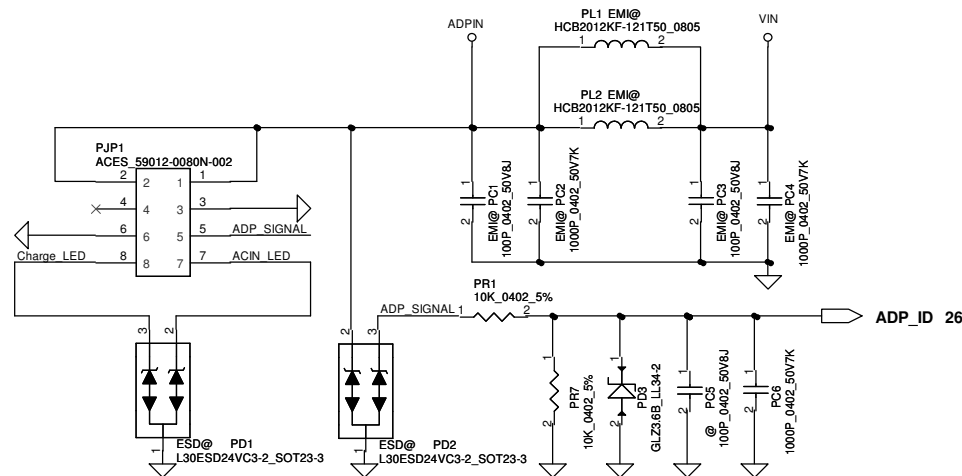
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				Friday, February 21, 2014	
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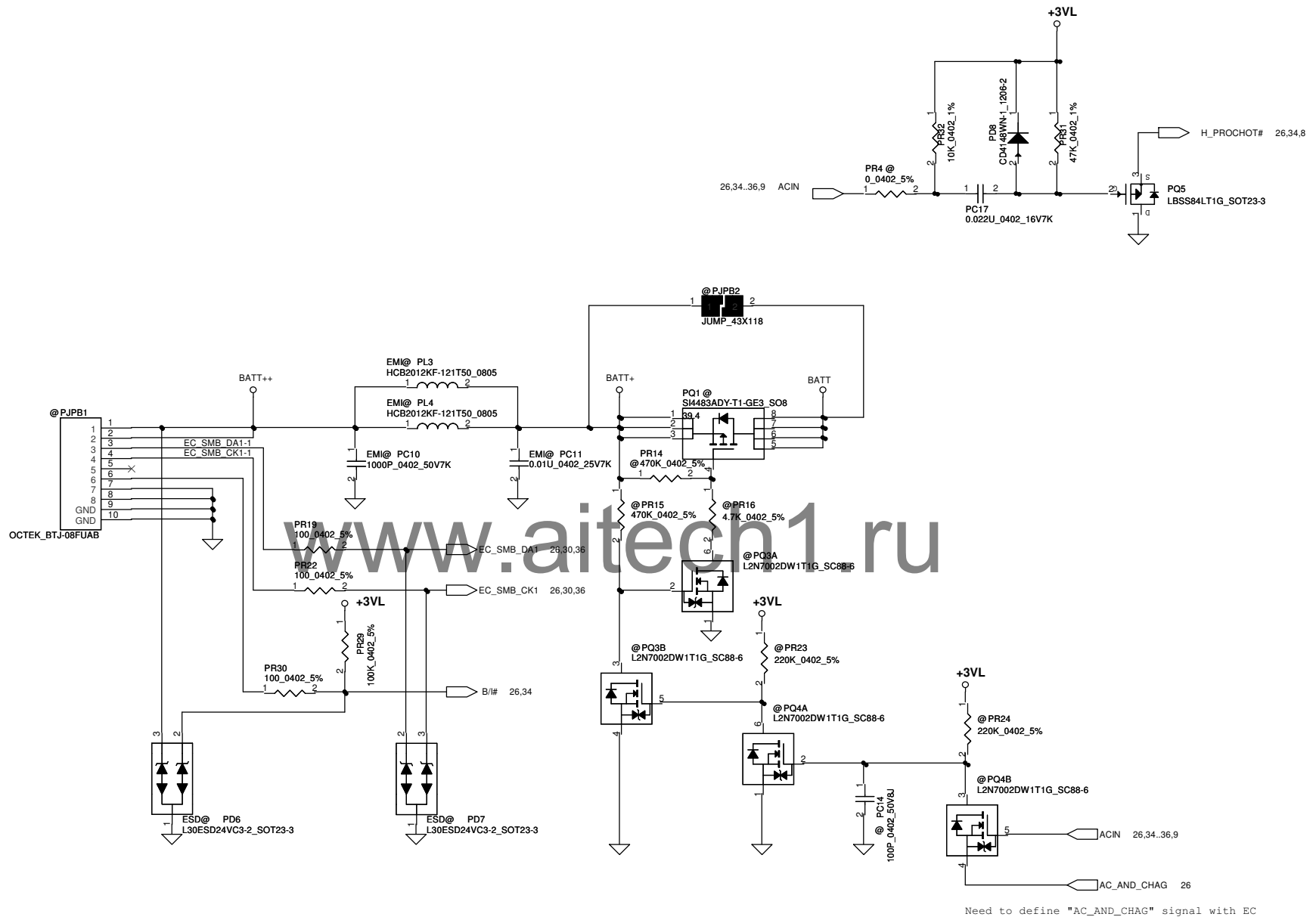




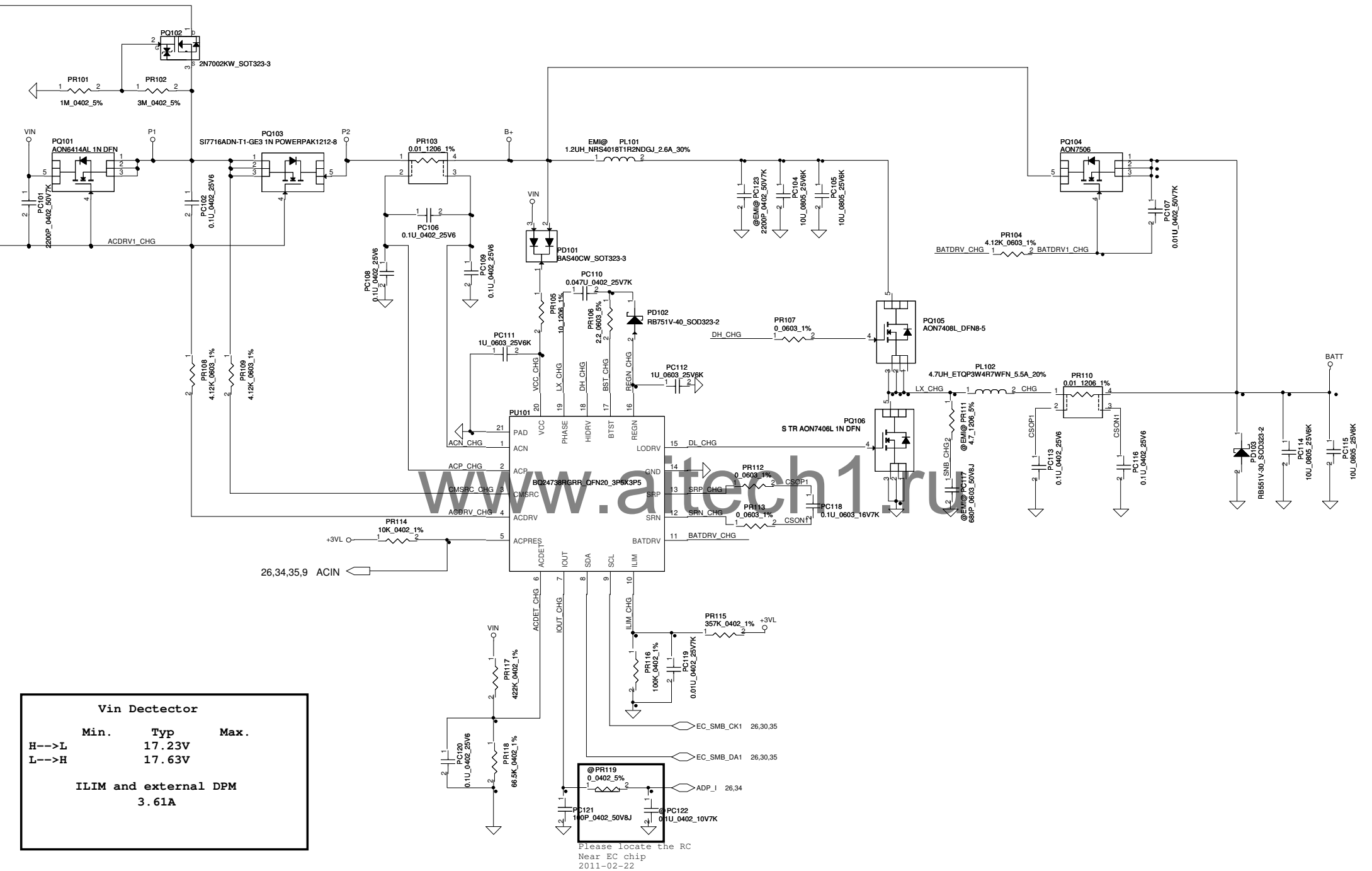
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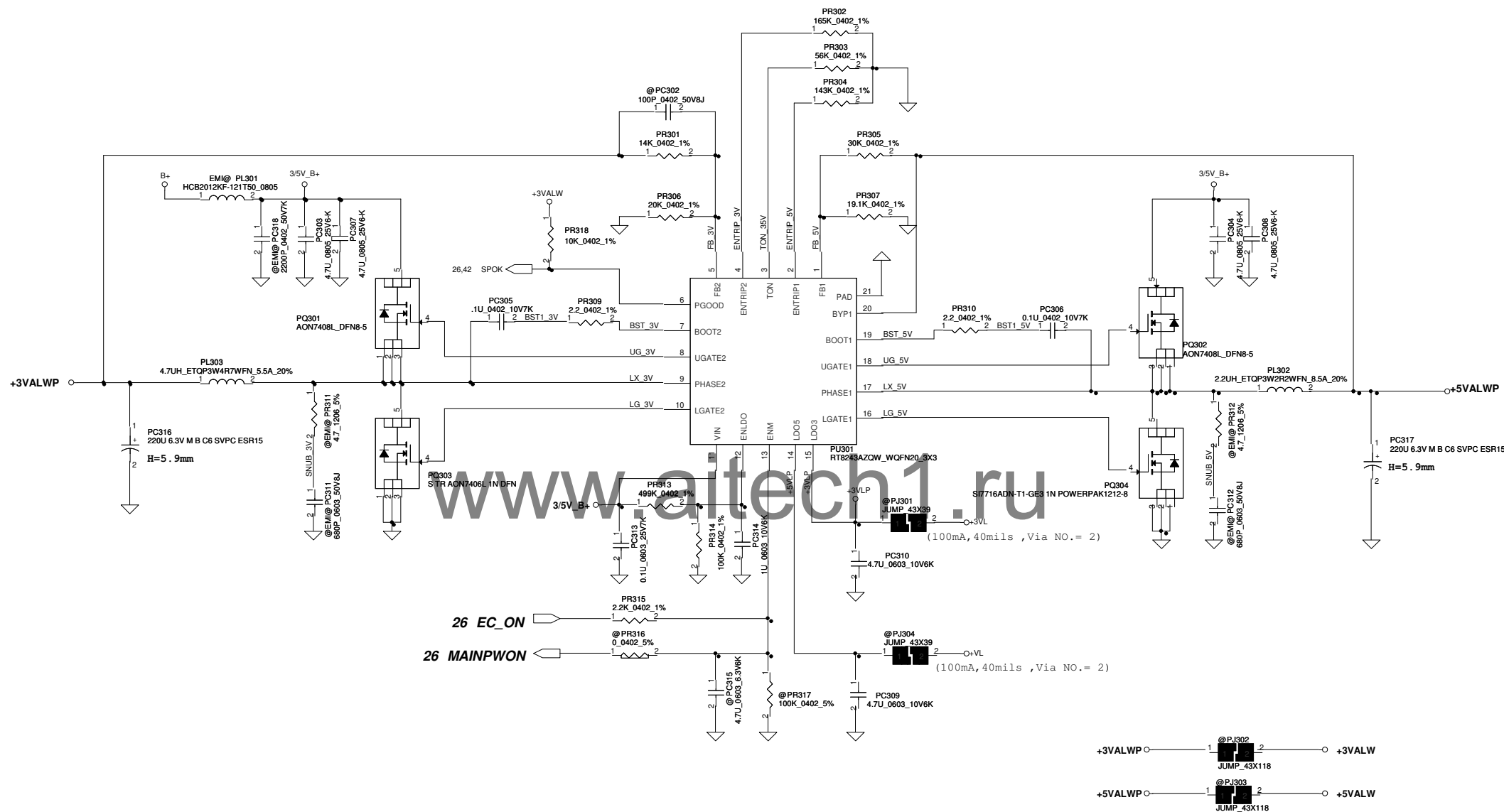
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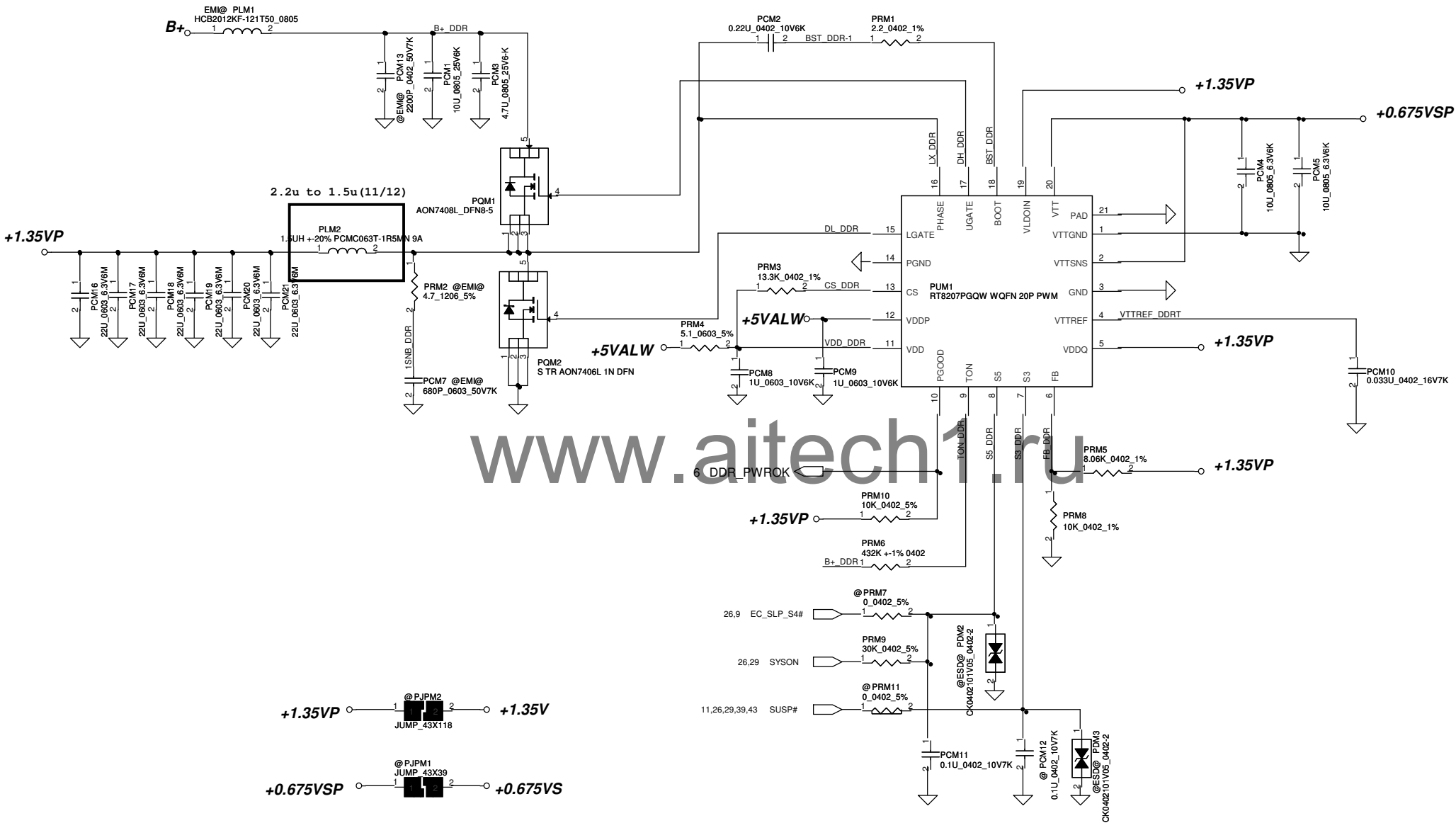
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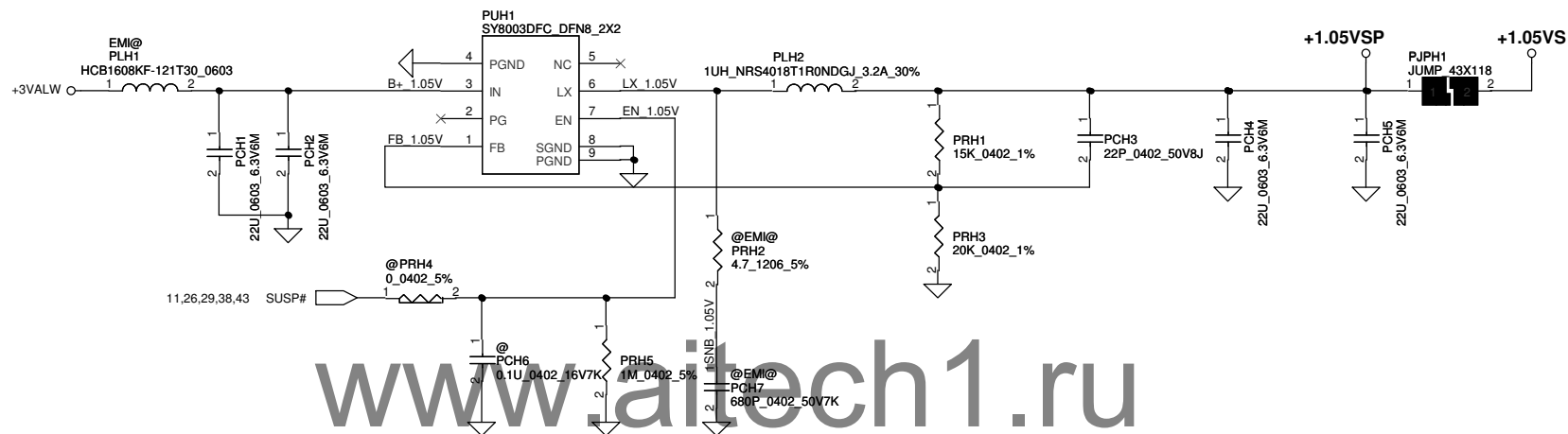
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GFX (GT2):  $I_{cc}=14A$   
Loadline:  $-5.9 \text{ m V/A}$

GFX (GT2):  $I_{cc}=14A$   
Loadline:  $-5.9 \text{ m V/A}$

For VR\_HOT#, already  
pull high at power side.

PR18 and PR30  
27.4K ohm for 100 degree  
61.9K ohm for 110 degree

1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
2. SVID spacing requirement is 18mil (0.475mm)   $\leq \text{SSSENSE}$
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mil (152.4mm).
4. The SVID bus must be ground reference. It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

**Layout Note**  
**Reduce Acoustic Noise**  
 1. The AL bulk capacitor of B+ should be very close to CPU\_CORE MOSFET.  
 2. Input ceramic caps must place on symmetry same location on top side and bottom side.

MDV1525  $V_{ds}=30V$   
 $R_{ds(on)}=11.5\sim 14m\ \Omega @ V_{gs}=4.5V$

UGA, GFX 1 2 UGA, GFX-1 4

PRG1 @ 0.0603, 5%

100V 10V 10V 2200V

OCP setting = ~20A

0.22uH DCR = 0.97 + 5% m ohm, Idc-Isat = 25-34A

MDU1511 Vds=30V  
Rds(on)=2.7~3.3m ohm@Vgs=4.5V

VDD source use +5VS and PGOOD source use +3VS  
Please confirm power on and down sequence,  
make sure VGATE after CPU CORE on.

MDV1525  $V_{ds}=30V$   
 $R_{ds(on)}=11.5\sim 14m\ \Omega @V_{gs}=4.5V$

MDU1511 Vds=30V  
Rds(on)=2.7~3.3m ohm@Vgs=4.5V

OCP setting= $\sim 18A$   
 $\sim T_{sat} = 25 \sim 34A$

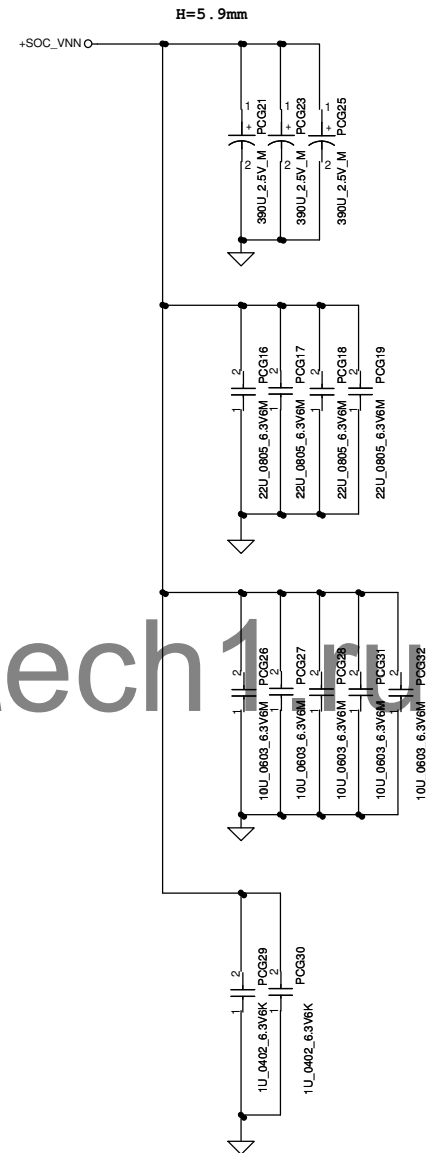
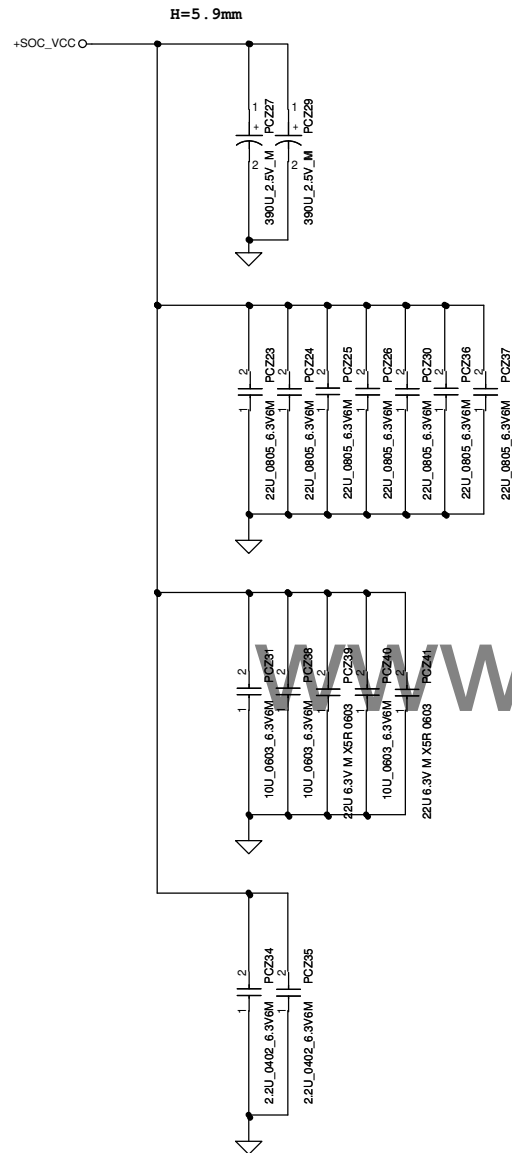
## Close CPU choke

$$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum})) * DCR$$

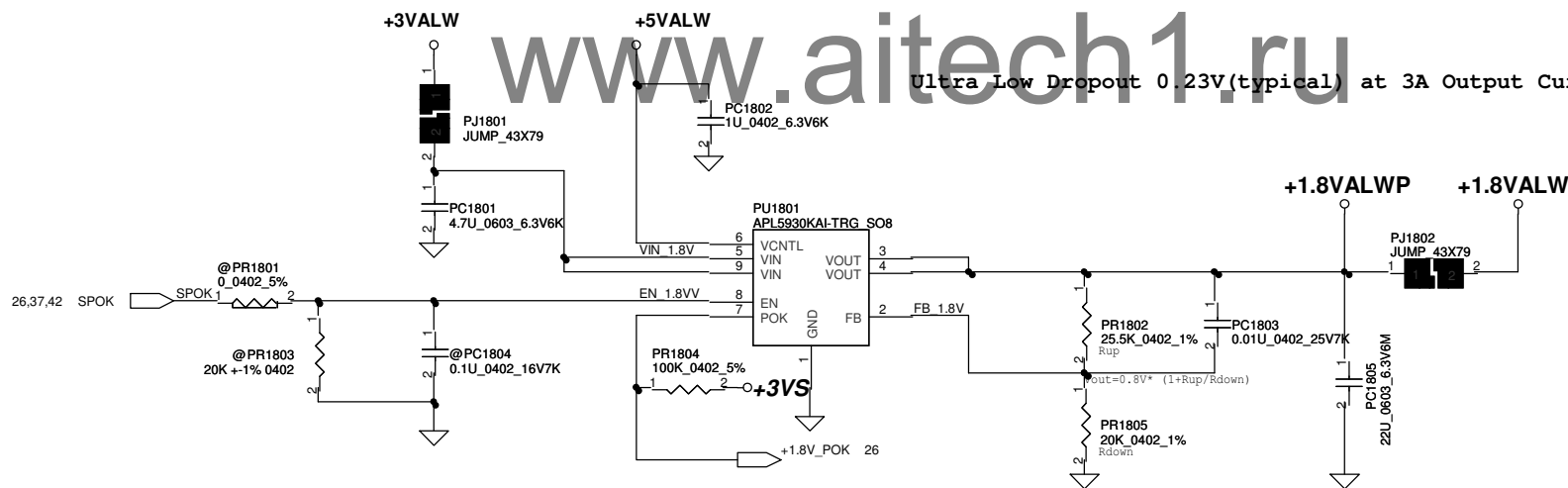
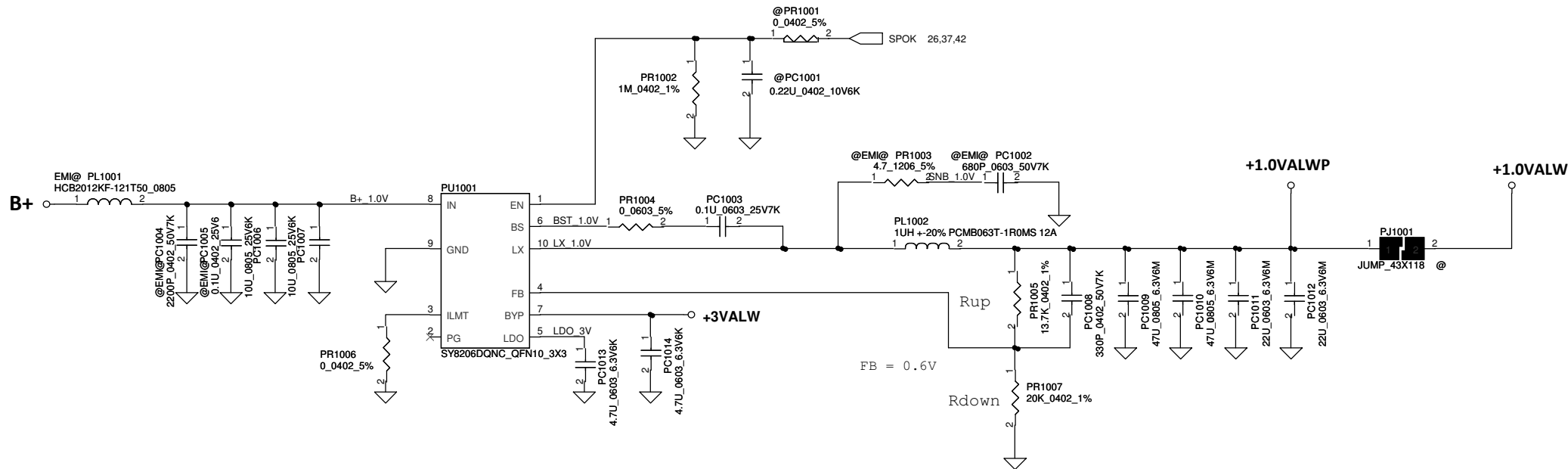
If  $C_n$  is correctly selected, when the load current has a square change, the output voltage also has a square response.

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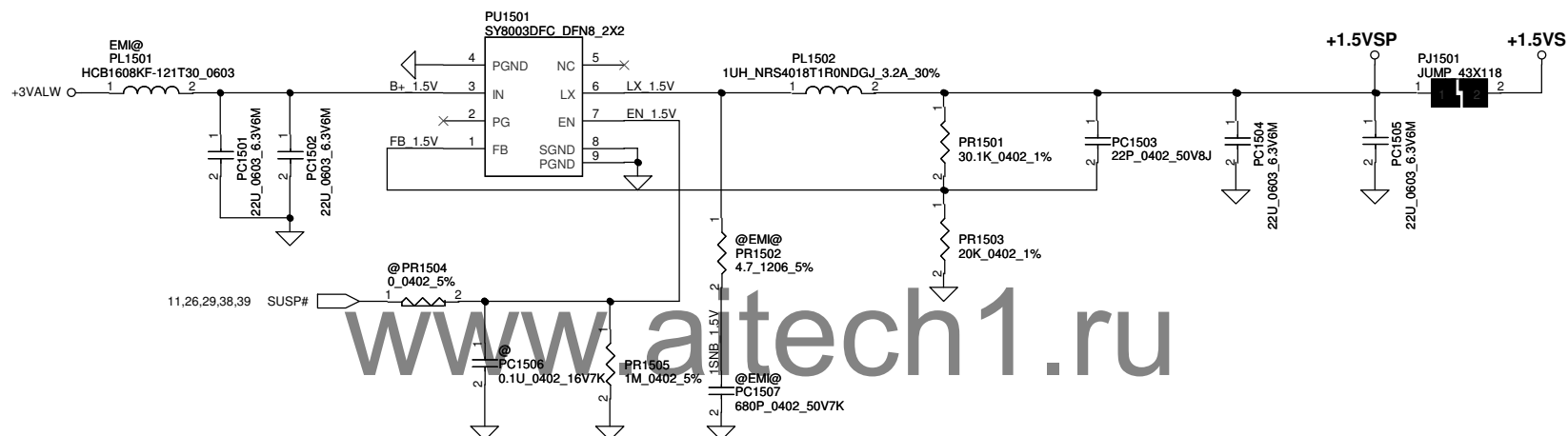




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